

LCFC Confidential

BALG1/AILG1/AILZ1 M/B Schematics Document


Intel Haswell U-Processor with DDRIIIL + NV (N15V-GM/N15S-GT) GPU

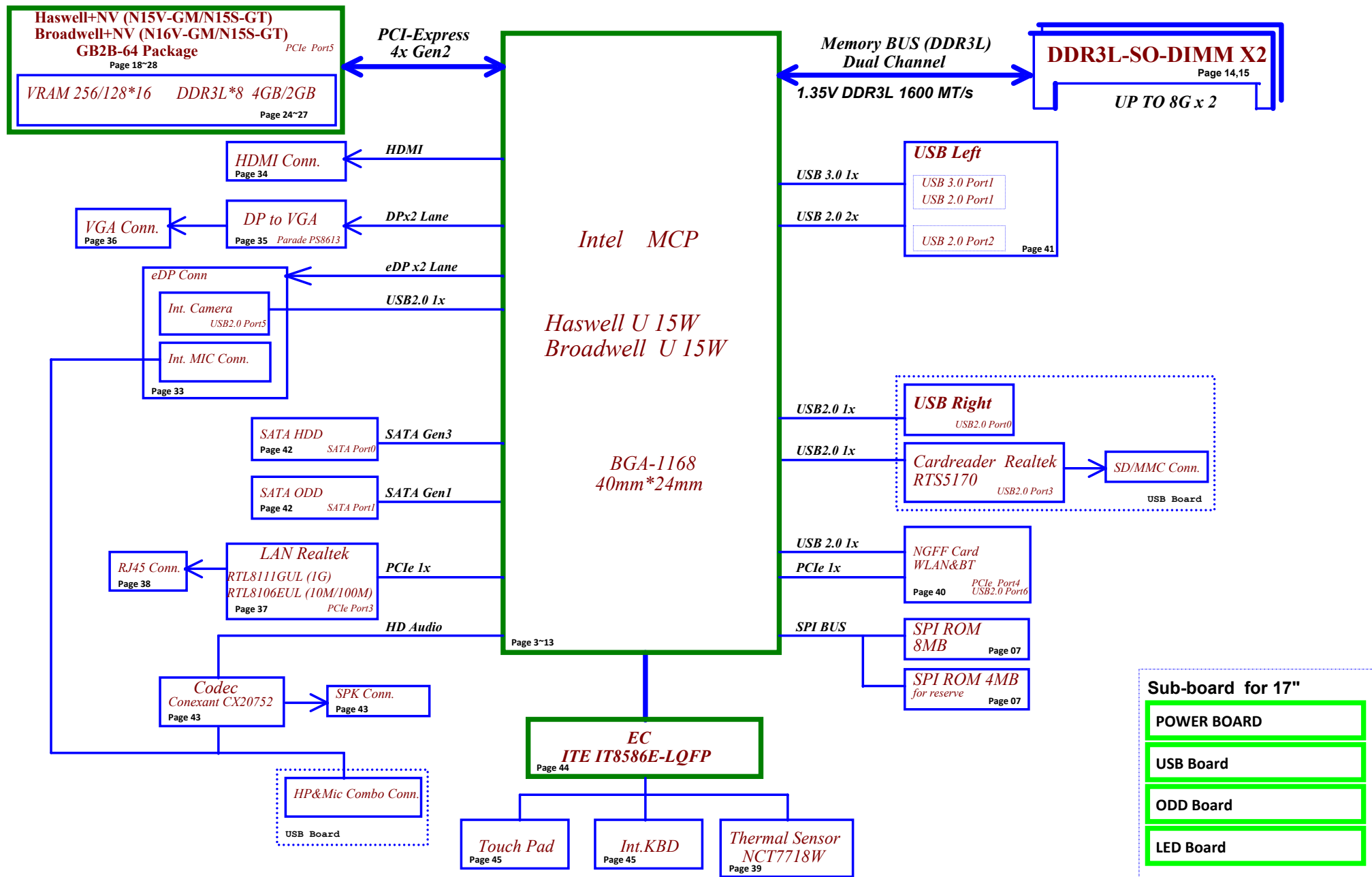
Intel Broadwell U-Processor with DDRIIIL + NV (N16V-GM/N15S-GT) GPU

MB: NMA331

2014-06-28

REV: 0.4

Security Classification	LC Future Center Secret Data			Title			
Issued Date	2014/06/28	Deciphered Date	2015/06/28	Cover Page			
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				Custom	BILG1/AILG1/AILZ1	0.4	
Date:				Wednesday, July 16, 2014		Sheet	1 of 60



Voltage Rails (O --> Means ON , X --> Means OFF)

<div>Power Plane</div> <div>State</div>	B+	<div>+3VALW</div> <div>+5VALW</div>	+3VALW_PCH	+1.35V	<div>+5VS</div> <div>+3VS</div> <div>+1.5VS</div> <div>+1.35VS</div> <div>+1.05VS</div> <div>+0.675VS</div> <div>CPU_CORE</div> <div>+VGA_CORE</div> <div>+3VGS</div> <div>+1.8VGS</div> <div>+1.35VGS</div> <div>+0.95VGS</div>
S0	○	○	○	○	○
S3	○	○	○	○	✗
S3 Battery only	○	○	○	○	✗
S5 S4/AC Only	○	○	○	✗	✗
S5 S4 Battery only	○	✗	✗	✗	✗
S5 S4 AC & Battery don't exist	✗	✗	✗	✗	✗

SMBUS Control Table

	SOURCE	VGA	BATT	IT8586E	SODIMM	WLAN WiMAX	Thermal Sensor	PCH	TP Module	charger
EC_SMB_CK1 EC_SMB_DA1	IT8586E +3VALW	X	V	V +3VALW	X	X	X	X	X	V
EC_SMB_CK2 EC_SMB_DA2	IT8586E +3VS	V +3VGS	X	V +3VS	X	X	V +3VS	V +3VALW_PCH	X	X
PCH_SMB_CLK PCH_SMB_DATA	PCH +3VALW_PCH	X	X	X	V +3VS	V +3VS	X	V +3VALW_PCH	X	X

EC SM Bus1 address		EC SM Bus2 address		PCH SM Bus address	
Device		Device	Address	Device	Address
Smart Battery	0X16	Thermal Sensor NCT7718W	1001_100xb	DDR DIMMA	1010 000Xb
Charger	0001 0010 b	VGA	0x41(default)	DDR DIMMB	1010 010Xb
		PCH	need to update	Wlan	Rsvd

STATE \ SIGNAL	SLP_S1#	SLP_S3#	SLP_S4#	SLP_S5#	+VALW	+V	+VS	Clock
Full ON	HIGH	HIGH	HIGH	HIGH	ON	ON	ON	ON
S1 (Power On Suspend)	LOW	HIGH	HIGH	HIGH	ON	ON	ON	LOW
S3 (Suspend to RAM)	LOW	LOW	HIGH	HIGH	ON	ON	OFF	OFF
S4 (Suspend to Disk)	LOW	LOW	LOW	HIGH	ON	OFF	OFF	OFF
S5 (Soft OFF)	LOW	LOW	LOW	LOW	ON	OFF	OFF	OFF

USB Port Table

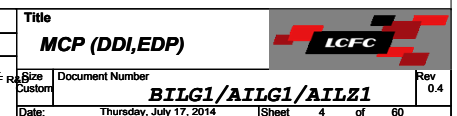
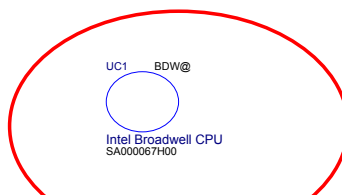
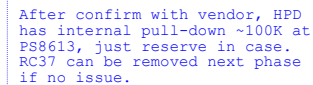
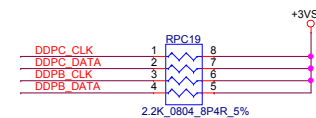
USB 2.0 EHCI1		USB 3.0 XHCI	
0	USB Port (Right Side)		
1	USB Port1 (Left Side)	1	USB Port1 (Left Side)
2	USB Port2 (Left Side)	2	
3	Cardreader	3	
4	TOUCH PANEL	4	
5	Camera		
6	NGFF(WLAN)		
7			

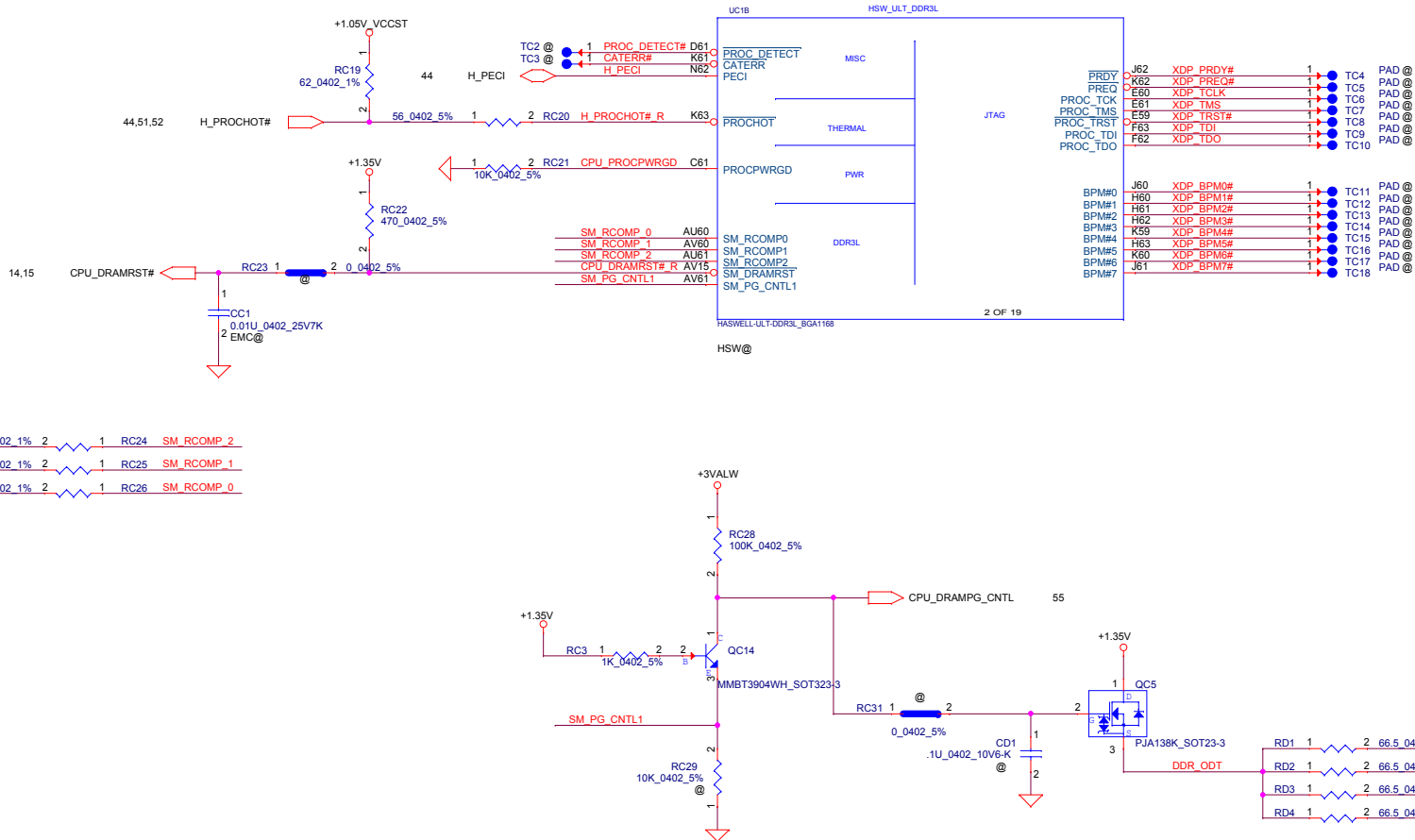
PCIE PORT LIST

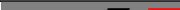
Port	Device
1	
2	
3	LAN
4	WLAN
5	Discrete GPU
6	

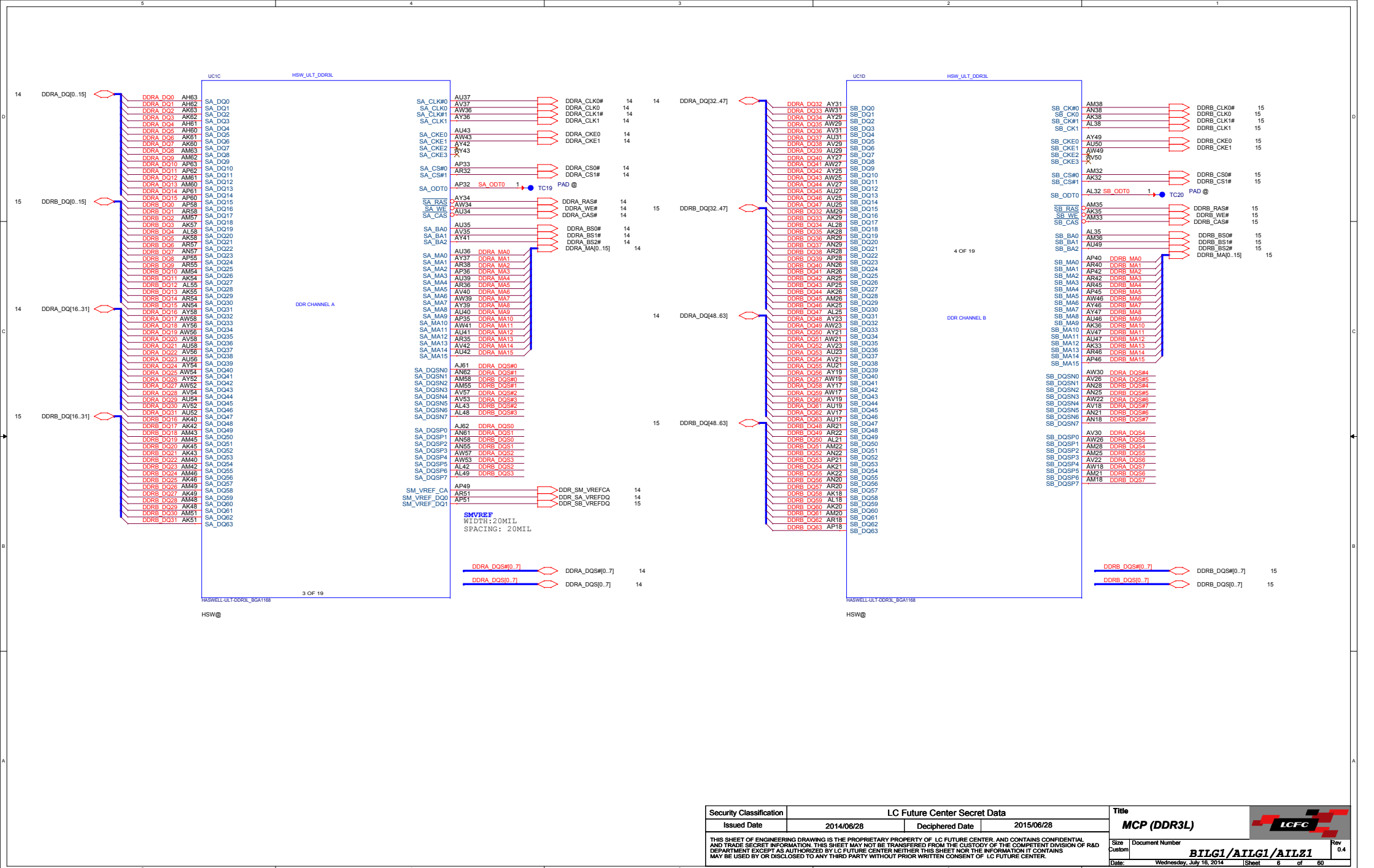
BOM Structure Table

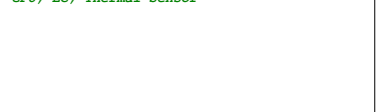
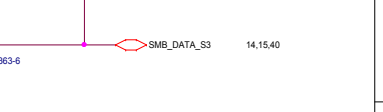
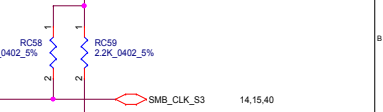
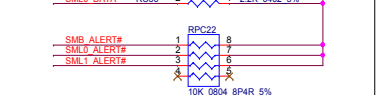
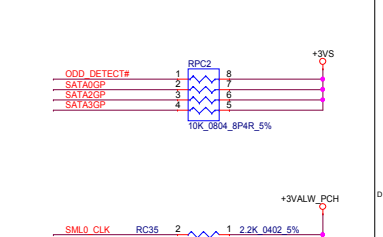
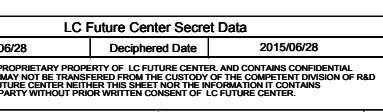
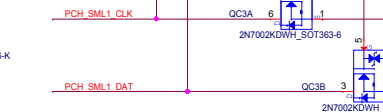
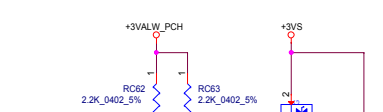
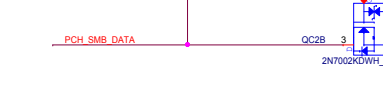
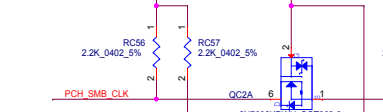
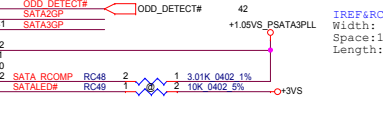
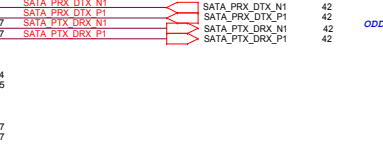
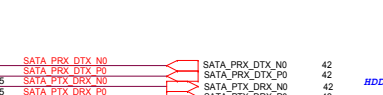
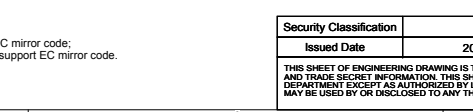
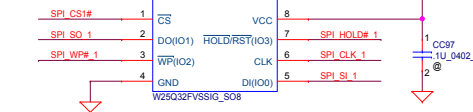
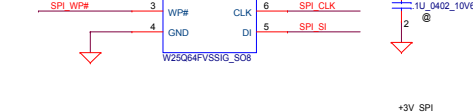
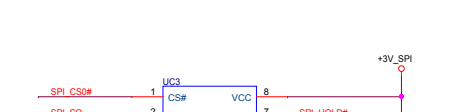
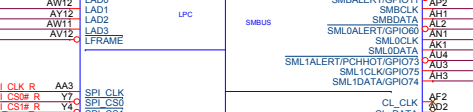
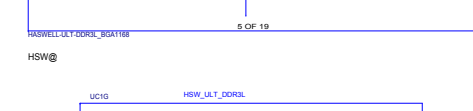
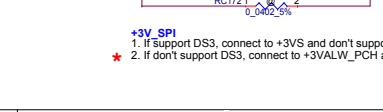
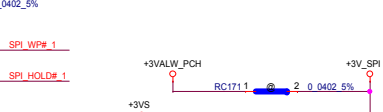
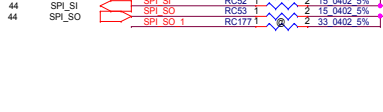
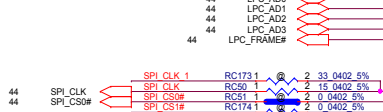
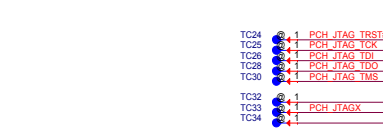
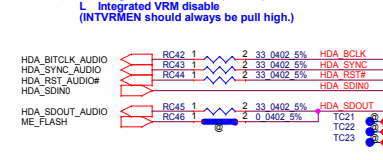
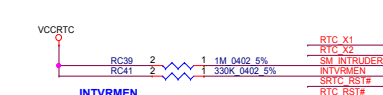
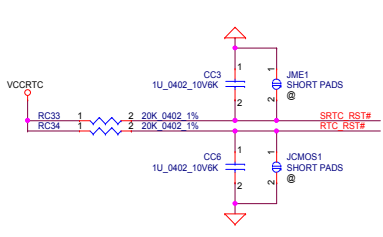
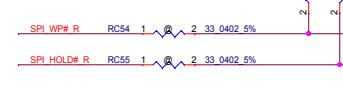
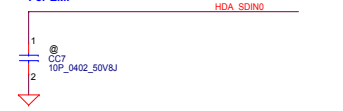
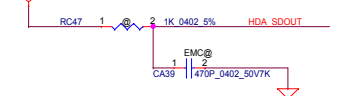
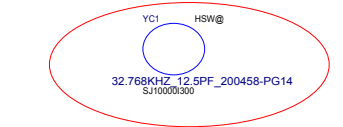
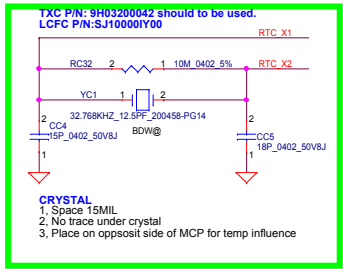
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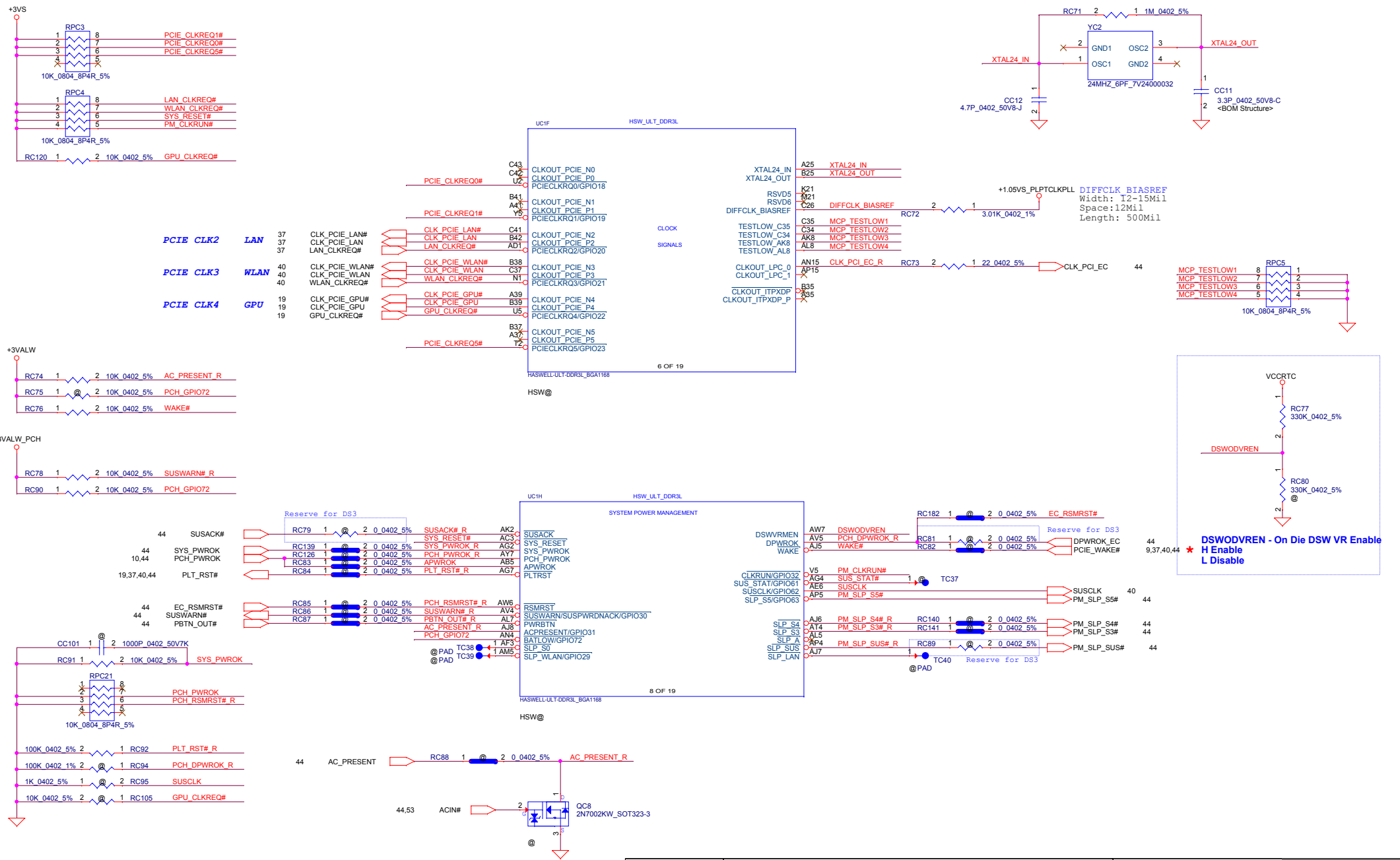





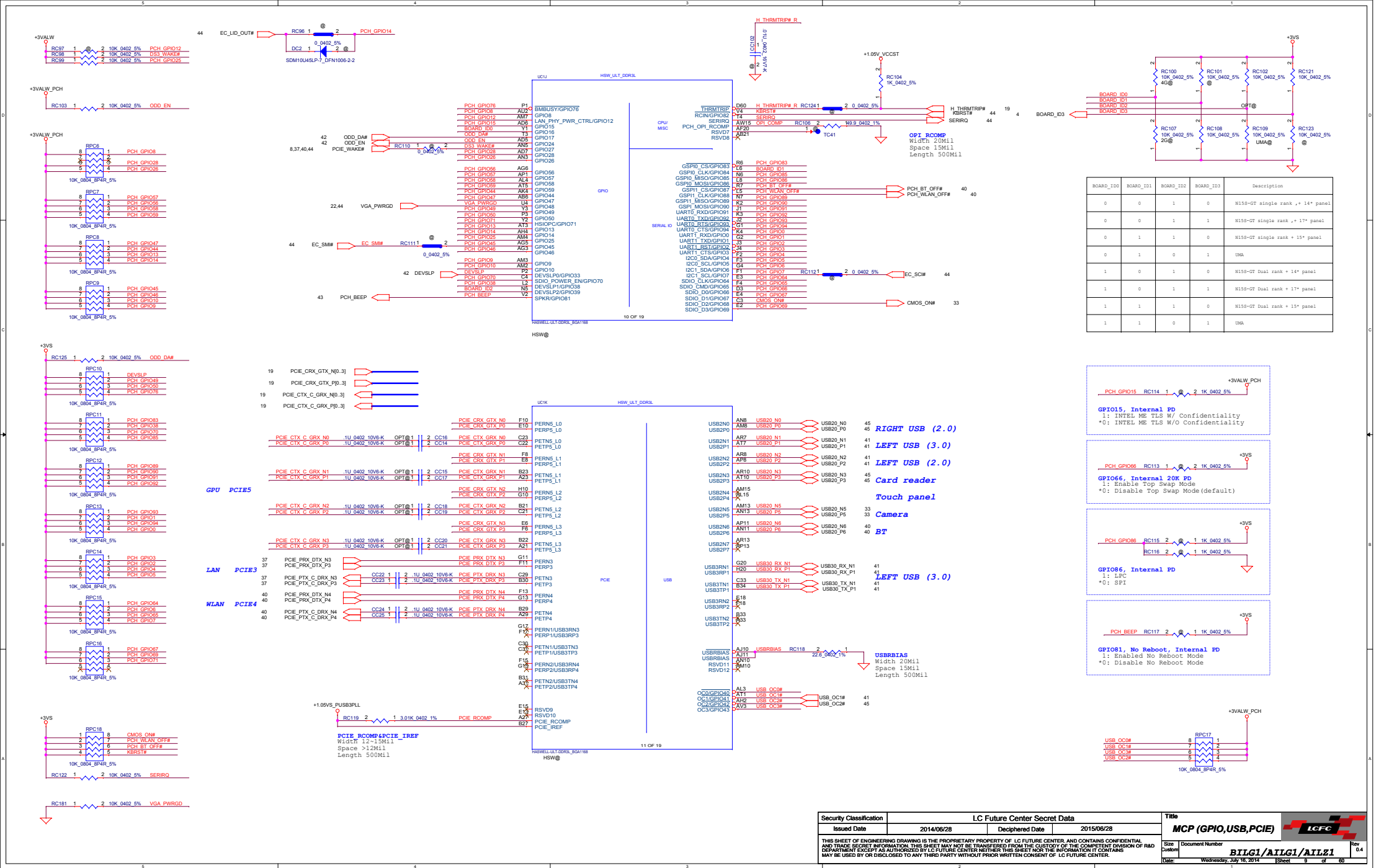
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Date:		Wednesday, July 16, 2014		Sheet 5 of 60		




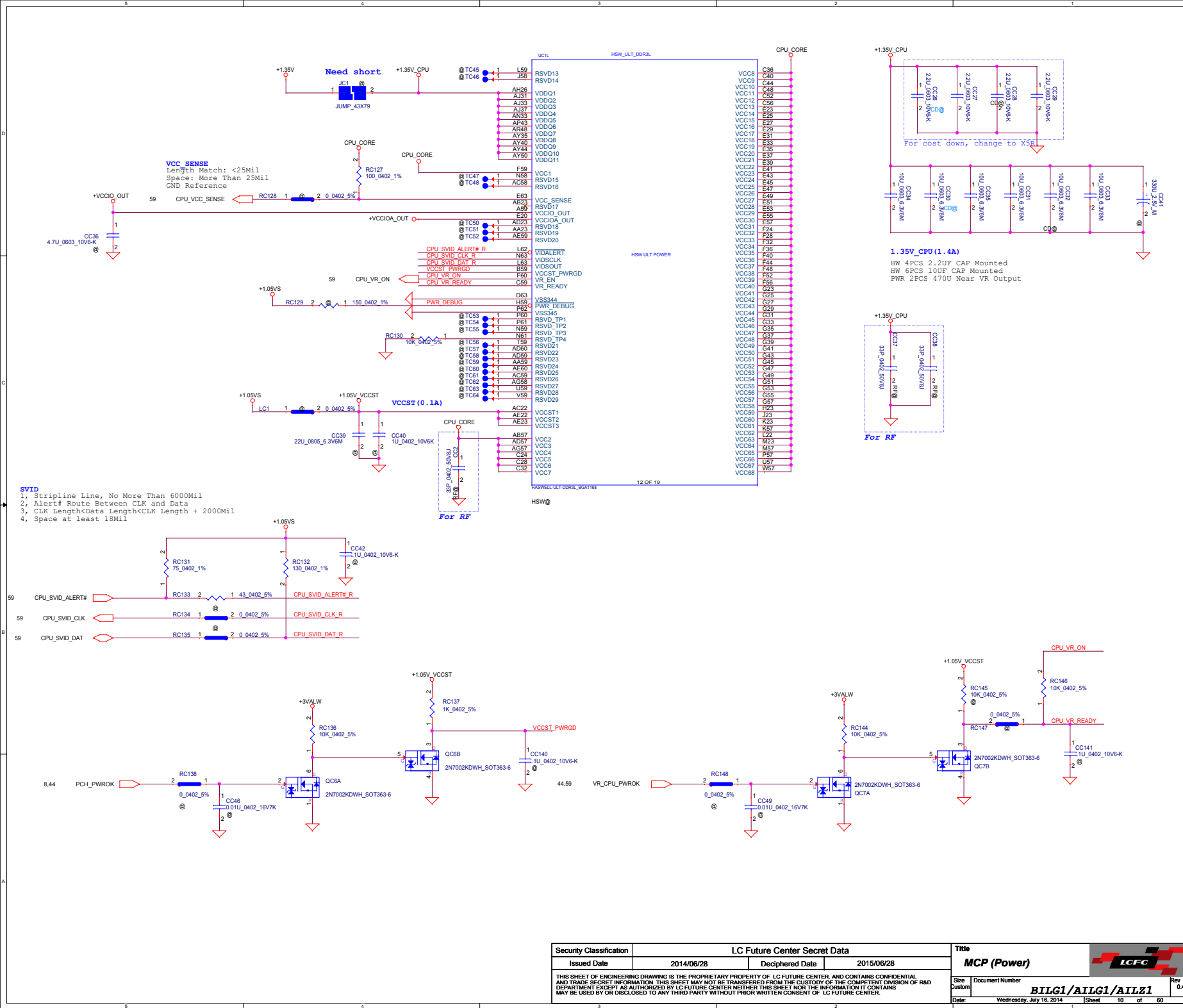


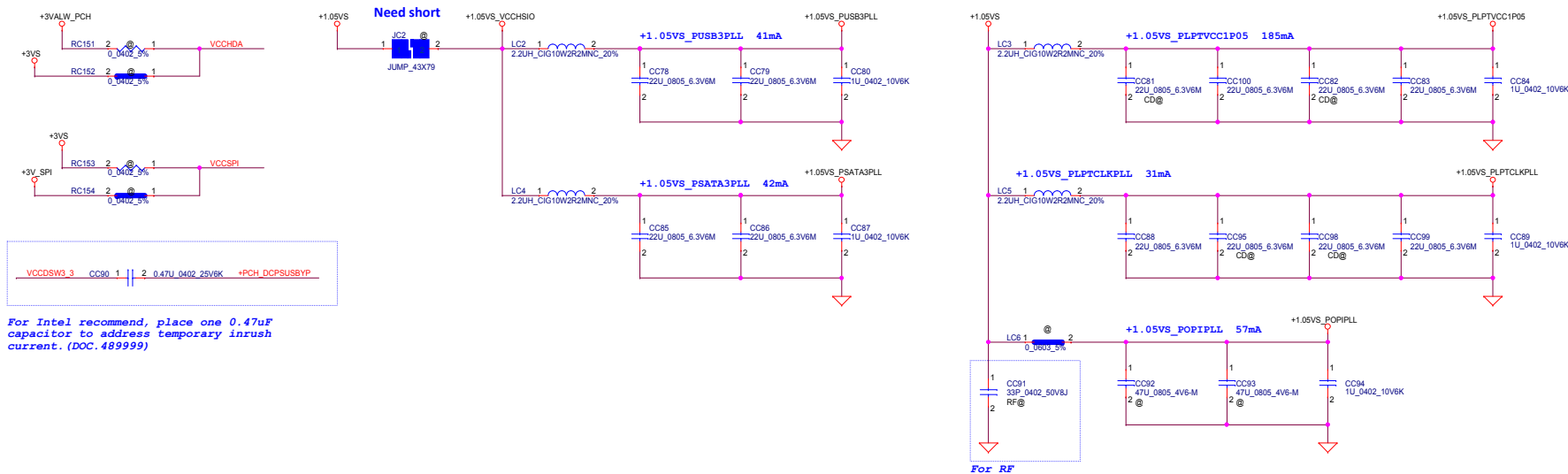



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								Sheet		8 of 60	
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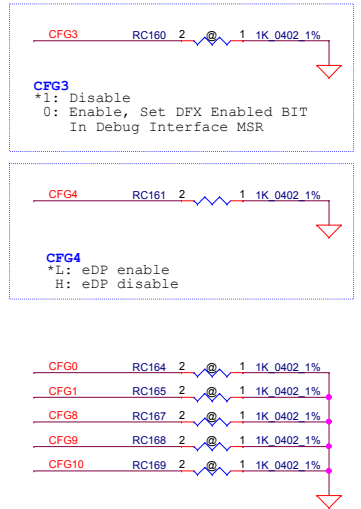
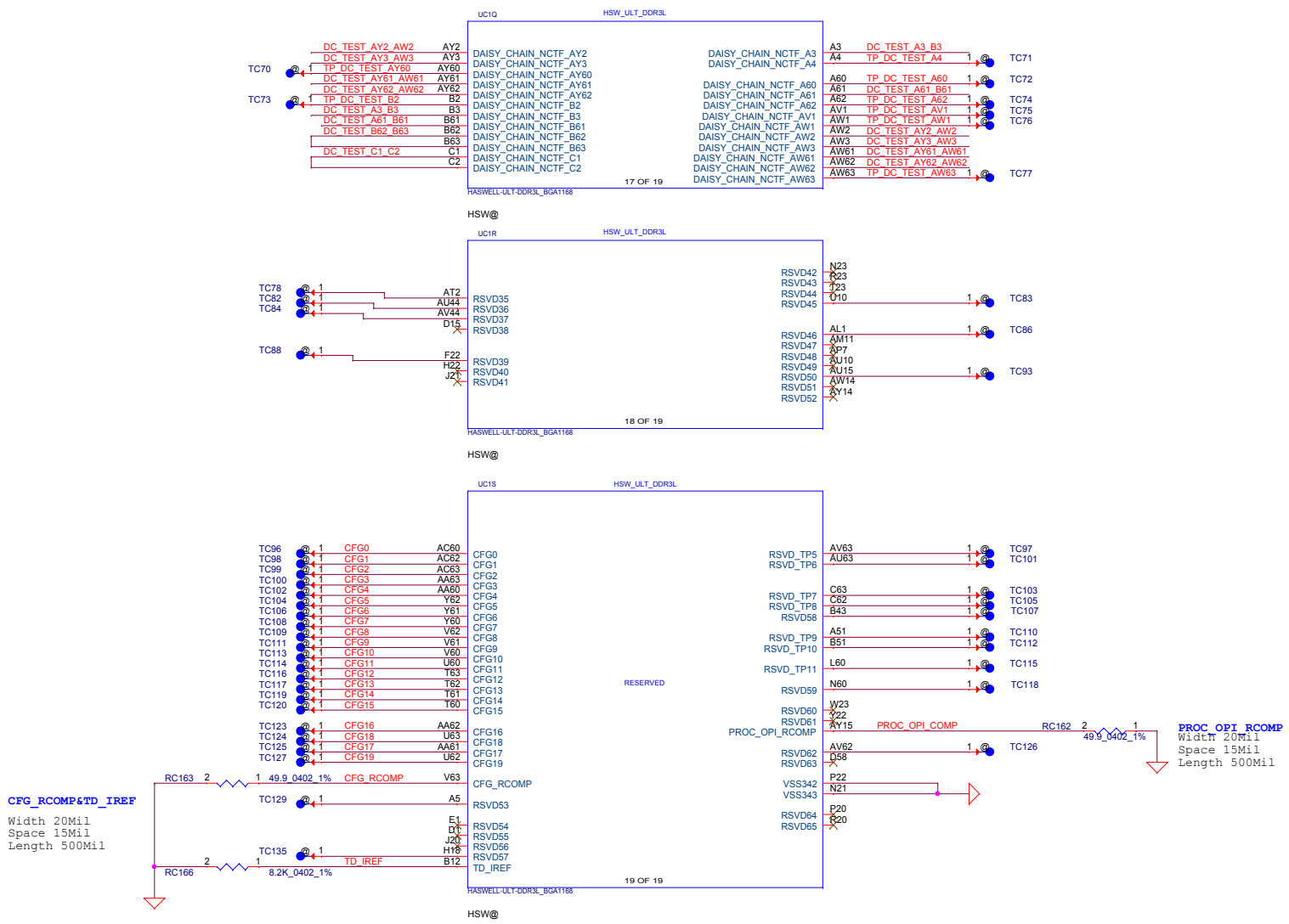


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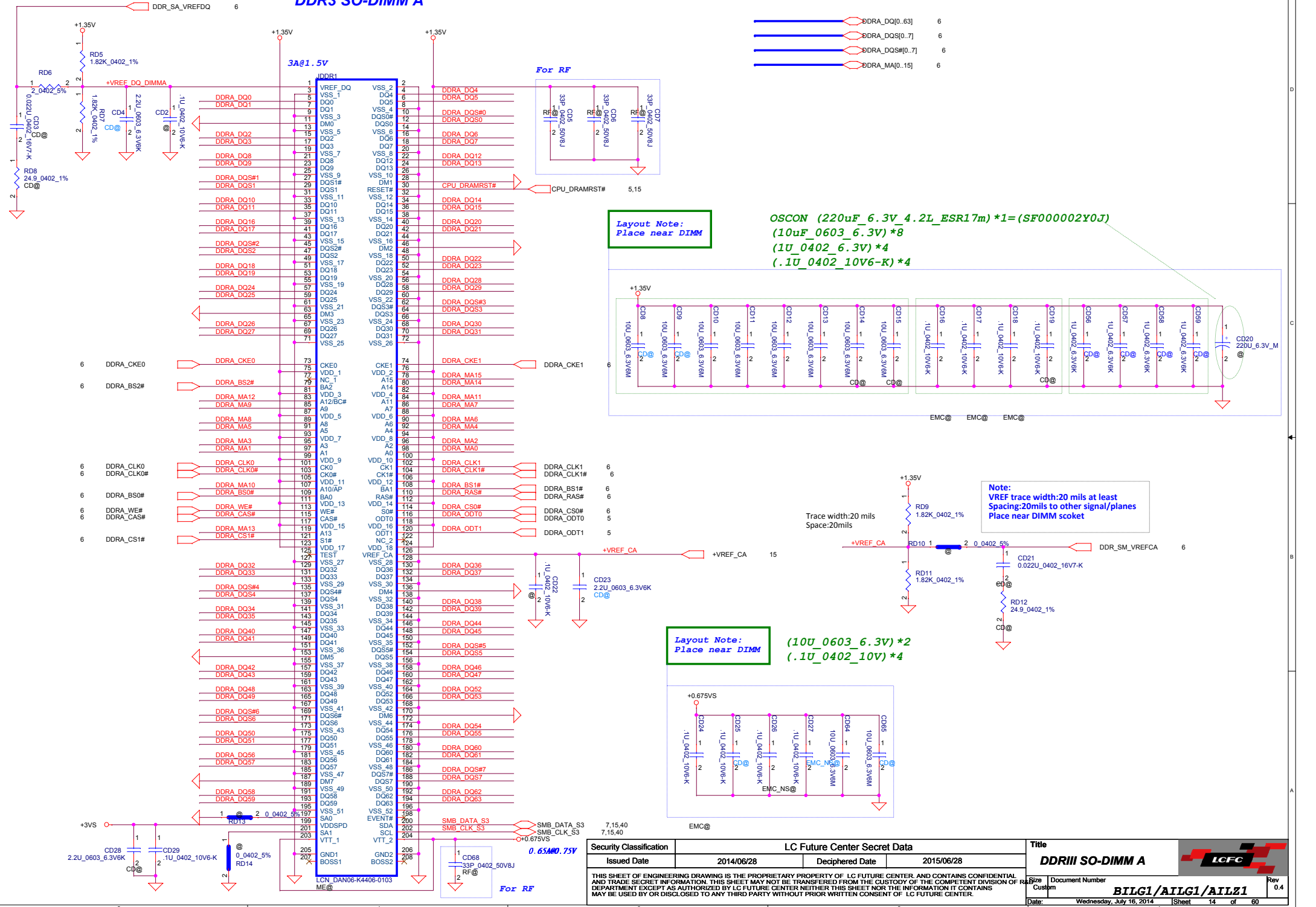


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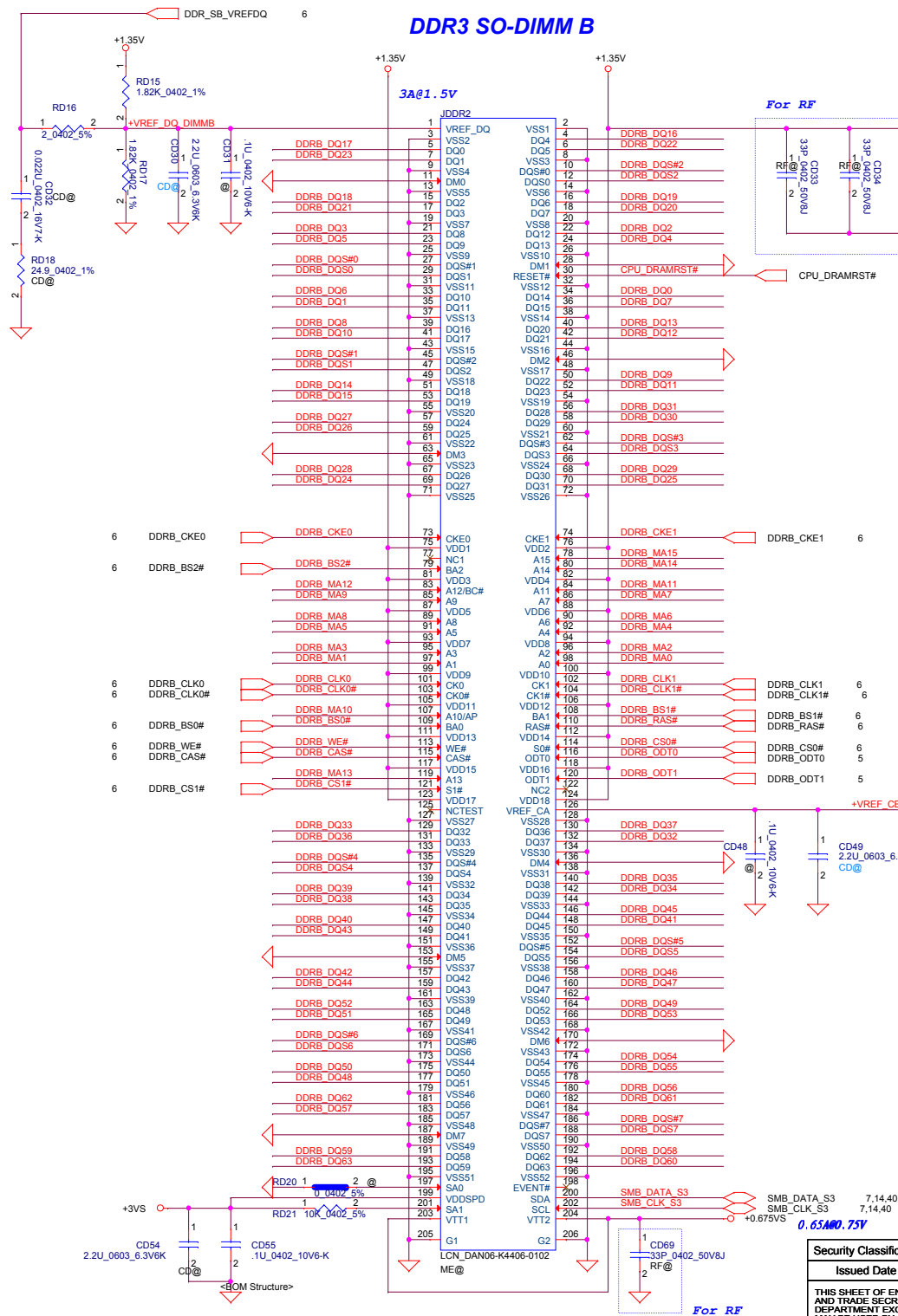
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Issued Date	2014/06/28	Deciphered Date	2015/06/28	MCP (OTHER)		
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Date:		Wednesday, July 16, 2014		Sheet	13	of 60
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DDR3 SO-DIMM A



DDR3 SO-DIMM B

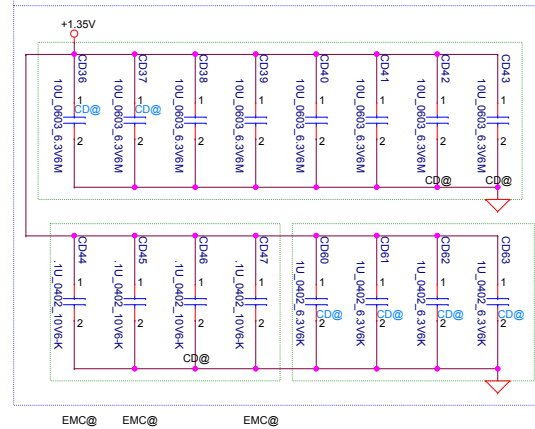


Swap Table

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15	DQ2	DDR3_DQ18
17	DQ3	DDR3_DQ21
4	DQ4	DDR3_DQ16
6	DQ5	DDR3_DQ22
16	DQ6	DDR3_DQ19
18	DQ7	DDR3_DQ20
10	DQS#0	DDR3_DQS#2
12	DQS0	DDR3_DQS2
21	DQ8	DDR3_DQ3
23	DQ9	DDR3_DQ5
33	DQ10	DDR3_DQ6
35	DQ11	DDR3_DQ1
22	DQ12	DDR3_DQ2
24	DQ13	DDR3_DQ4
34	DQ14	DDR3_DQ0
36	DQ15	DDR3_DQ7
27	DQS#1	DDR3_DQS#0
29	DQS1	DDR3_DQS0
39	DQ16	DDR3_DQ8
41	DQ17	DDR3_DQ10
51	DQ18	DDR3_DQ14
53	DQ19	DDR3_DQ15
40	DQ20	DDR3_DQ13
42	DQ21	DDR3_DQ12
50	DQ22	DDR3_DQ9
52	DQ23	DDR3_DQ11
45	DQS#2	DDR3_DQS#1
47	DQS2	DDR3_DQS1
57	DQ24	DDR3_DQ27
59	DQ25	DDR3_DQ26
67	DQ26	DDR3_DQ28
69	DQ27	DDR3_DQ24
56	DQ28	DDR3_DQ31
58	DQ29	DDR3_DQ30
68	DQ30	DDR3_DQ29
70	DQ31	DDR3_DQ25
62	DQS#3	DDR3_DQS#3
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132	DQ37	DDR3_DQ32
140	DQ38	DDR3_DQ35
142	DQ39	DDR3_DQ34
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147	DQ40	DDR3_DQ40
149	DQ41	DDR3_DQ43
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148	DQ45	DDR3_DQ41
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160	DQ47	DDR3_DQ47
152	DQS#5	DDR3_DQS#5
154	DQS5	DDR3_DQS5
163	DQ48	DDR3_DQ52
165	DQ49	DDR3_DQ51
175	DQ50	DDR3_DQ50
177	DQ51	DDR3_DQ48
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166	DQ53	DDR3_DQ53
174	DQ54	DDR3_DQ54
176	DQ55	DDR3_DQ55
169	DQS#6	DDR3_DQS#6
171	DQS6	DDR3_DQS6
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194	DQ63	DDR3_DQ60
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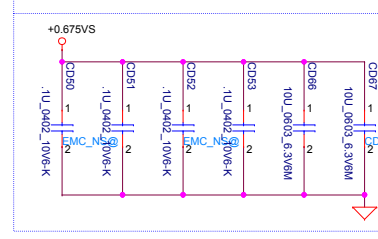
Layout Note:
Place near DIMM

(10uF_0603_6.3V)*8
(1U_0402_6.3V)*8
(.1U_0402_10V6-K)*4



Layout Note:
Place near DIMM

(10U_0603_6.3V)*2
(.1U_0402_10V)*4



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DDR3 SO-DIMM B	BALG1/AIGL1/AILE1	0.4
Date:	Wednesday, July 16, 2014	Sheet 15 of 60

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C				C					
B				B					
A				A					
		Security Classification		LC Future Center Secret Data		Title			
		Issued Date		2014/06/28		Deciphered Date		2015/06/28	
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				Date:		Wednesday, July 16, 2014		Sheet 16 of 60	
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				Date:		Wednesday, July 16, 2014		Sheet 17 of 60	
5	4	3	2	1					



N15x GPIO

GPIO	I/O	ACTIVE	Function Description
GPIO0	OUT	-	FB Enable for GC6 2.0
GPIO1	OUT	N/A	
GPIO2	OUT	N/A	
GPIO3	OUT	N/A	
GPIO4	OUT	N/A	
GPIO5	OUT	N/A	GPU power sequencing--3V3_MAIN_EN
GPIO6	IN	-	GPU wake signal for GC6 2.0
GPIO7	OUT	N/A	
GPIO8	I/O	-	System side PCIe reset Monitor
GPIO9	I/O	N/A	2.2K Pull-up
GPIO10	OUT	N/A	
GPIO11	OUT	-	GPU Core VDD PWM control signal
GPIO12	IN		AC Power Detect Input (10K pull High)
GPIO13	OUT	-	Phase Shedding
GPIO14	IN	N/A	
GPIO15	IN	N/A	
GPIO16		N/A	
GPIO17	IN	N/A	
GPIO18	IN	N/A	
GPIO19	IN	N/A	
GPIO20		N/A	
GPIO21	OUT		GPU PCIe self-reset control
OVERT	OUT		Active Low Thermal Catastrophic Over Temperature

Performance Mode P0 TDP at Tj = 102 C* (DDR3)

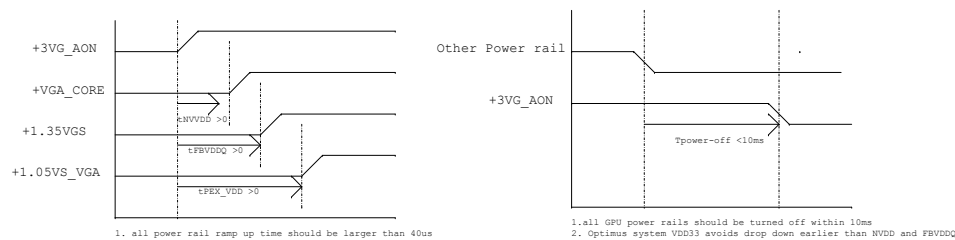
[illegible]

N15x Multi-level Straps

Physical Strapping pin	Power Rail	Logical Strapping Bit3	Logical Strapping Bit2	Logical Strapping Bit1	Logical Strapping Bit0
ROM_SCLK	+3VGS	SOR3_EXPOSED	SOR2_EXPOSED	SOR1_EXPOSED	SOR0_EXPOSED
ROM_SI	+3VGS	RAM_CFG[3]	RAM_CFG[2]	RAM_CFG[1]	RAM_CFG[0]
ROM_SO	+3VGS	DEVID_SEL	PCIE_CFG	SMB_ALT_ADDR	VGA_DEVICE
STRAP0	+3VGS	Reserved(keep pull-up and pull-down footprint and stuff 50Kohm pull-up)			
STRAP1	+3VGS				
STRAP2	+3VGS				
STRAP3	+3VGS	Reserved(keep pull-up and pull-down footprint and not stuff by default)			
STRAP4	+3VGS				

SMBUS_ALT_ADDR	
0	0x9E (Default)
1	0x9C (Multi-GPU usage)

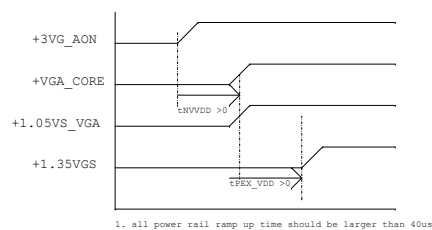
N15V-GM/N16V-GM Power Sequence




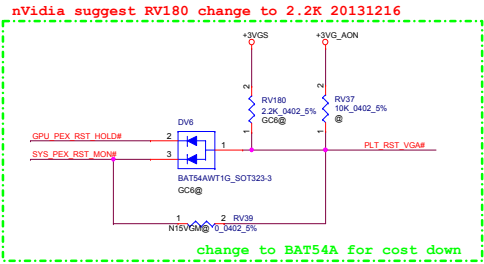
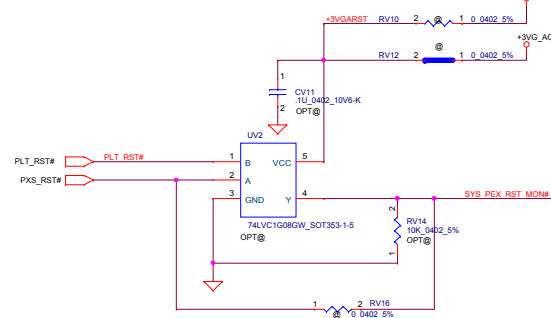
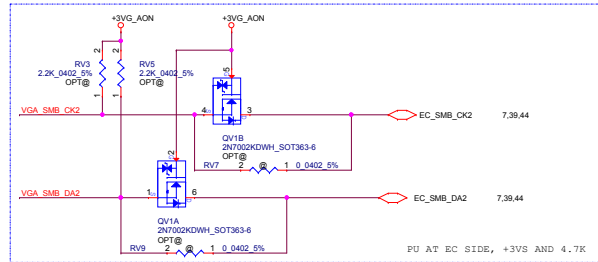
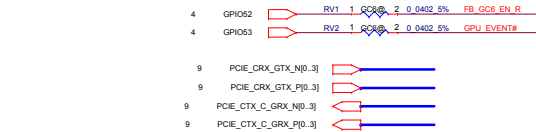
N15x Binary Straps

Physical Strapping pin	Power Rail	Strap Mapping
ROM_SCLK	+3VGS	SMB_ALT_ADDR
ROM_SI	+3VGS	SUB_VENDOR
ROM_SO	+3VGS	VGA_DEVICE
STRAP0	+3VGS	RAM_CFG[0]
STRAP1	+3VGS	RAM_CFG[1]
STRAP2	+3VGS	RAM_CFG[2]
STRAP3	+3VGS	RAM_CFG[3]
STRAP4	+3VGS	PCIEX_MAX_SPEED

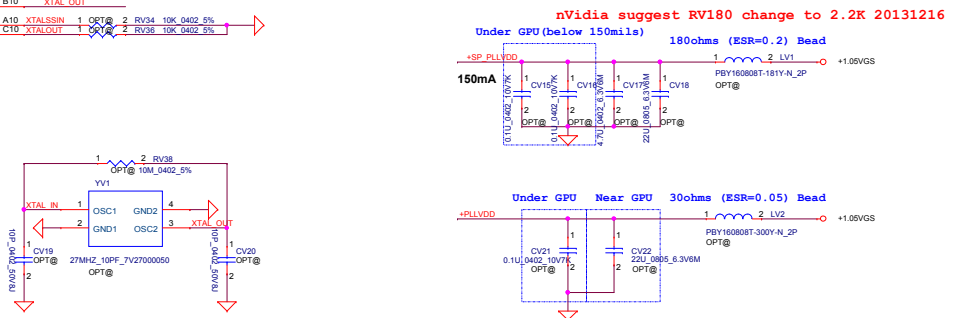
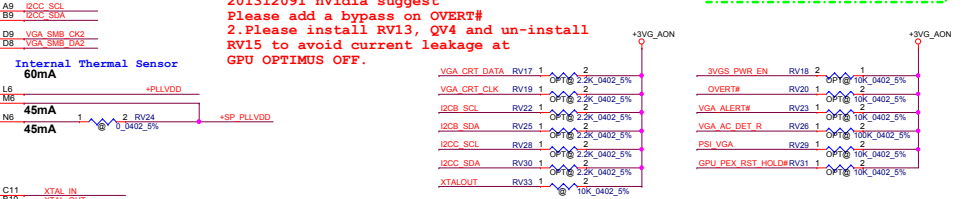
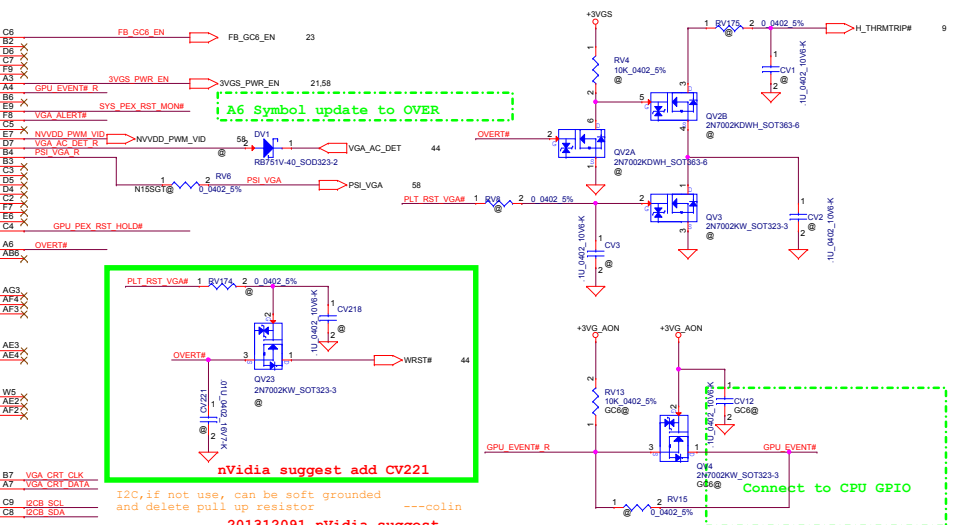
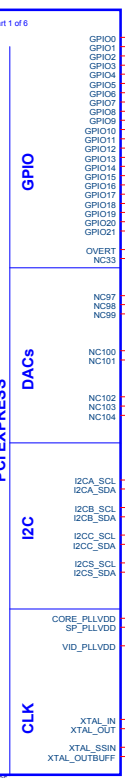
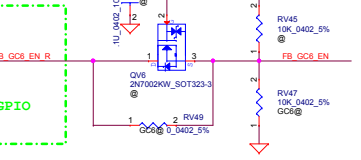
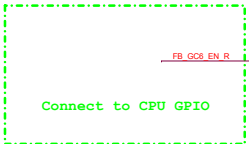
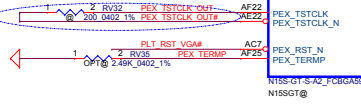
N15S-GT Power Sequence



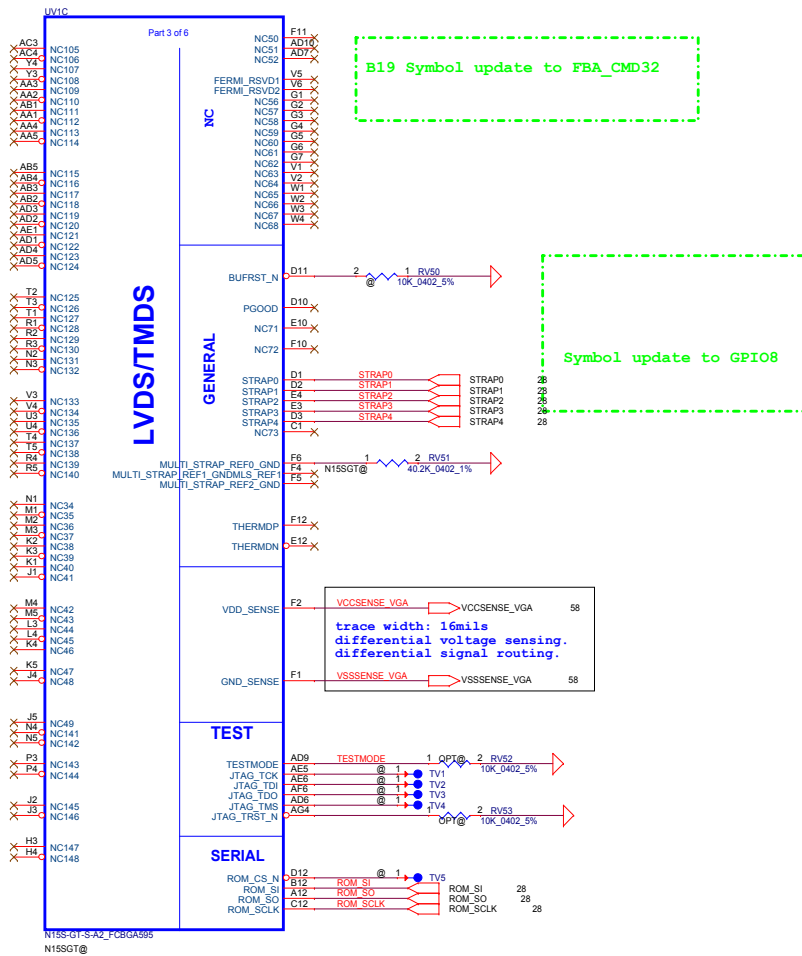
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Date:		Wednesday, July 16, 2014		ISheet 18 of 60		

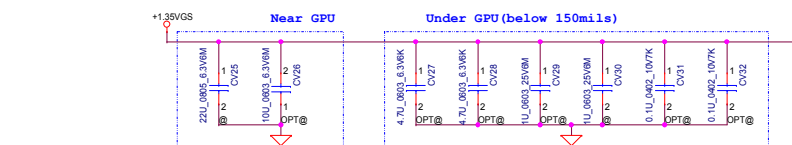


Differential signal



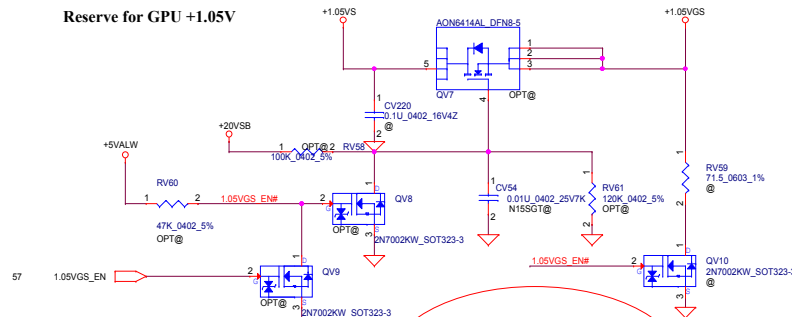
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				Date	Thursday, July 17, 2014
				Sheet	19 of 60





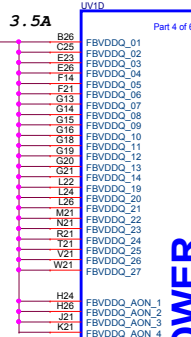
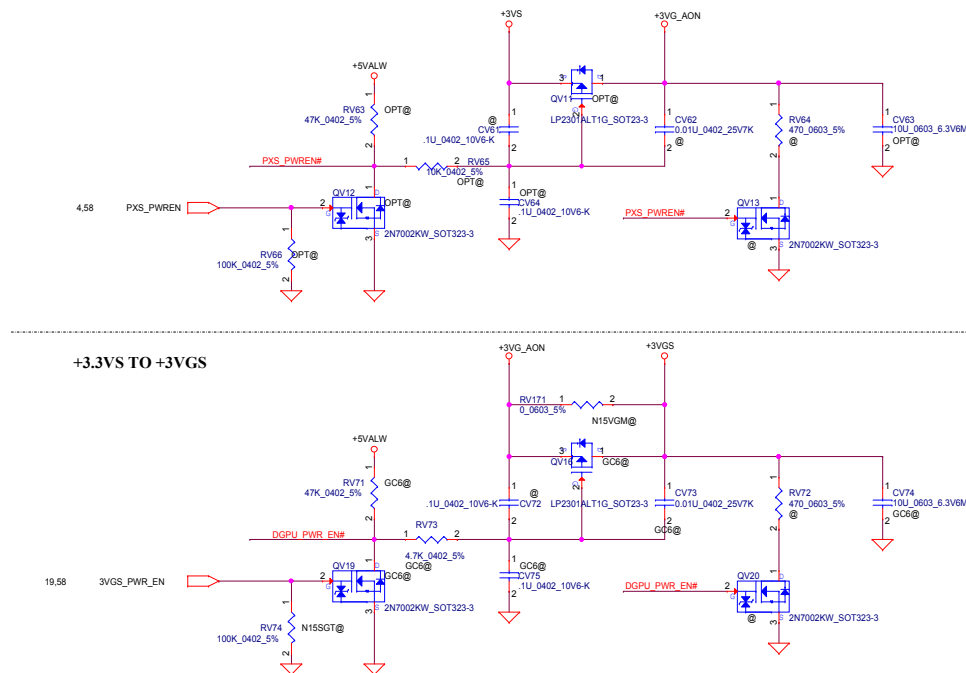
Symbol update to FBVDDQ_AON
H24/H26/J21/K21

Reserve for GPU +1.05V

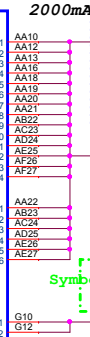


+3.3VS TO +3VG_AON

follow NV GPU rise time

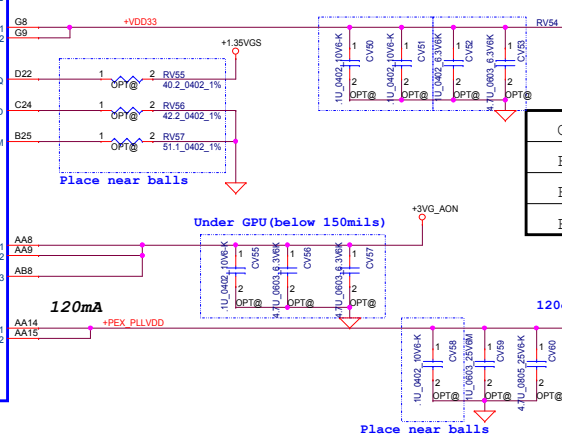


POWER



Symbol update to 3V3_AON

Place near balls (Under GPU) Place near GPU



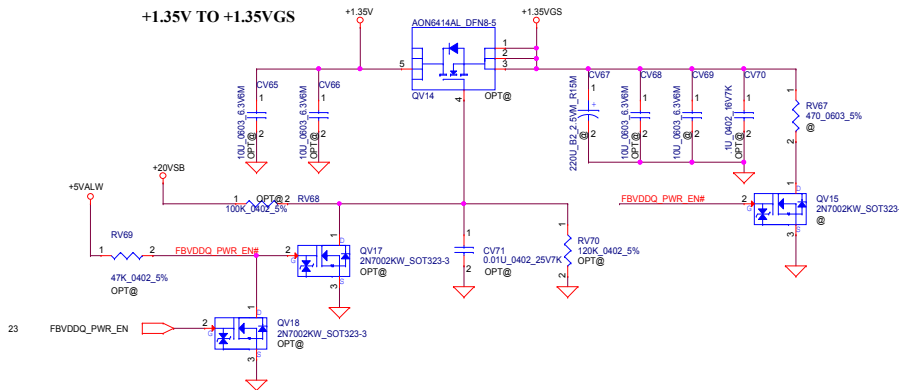
PEX_IOVDD/Q Decoupling

MLCC	N15V-GM	N15S-GT
1.0uF	4	1
4.7uF	2	1
10uF	4	1
22uF	4	1

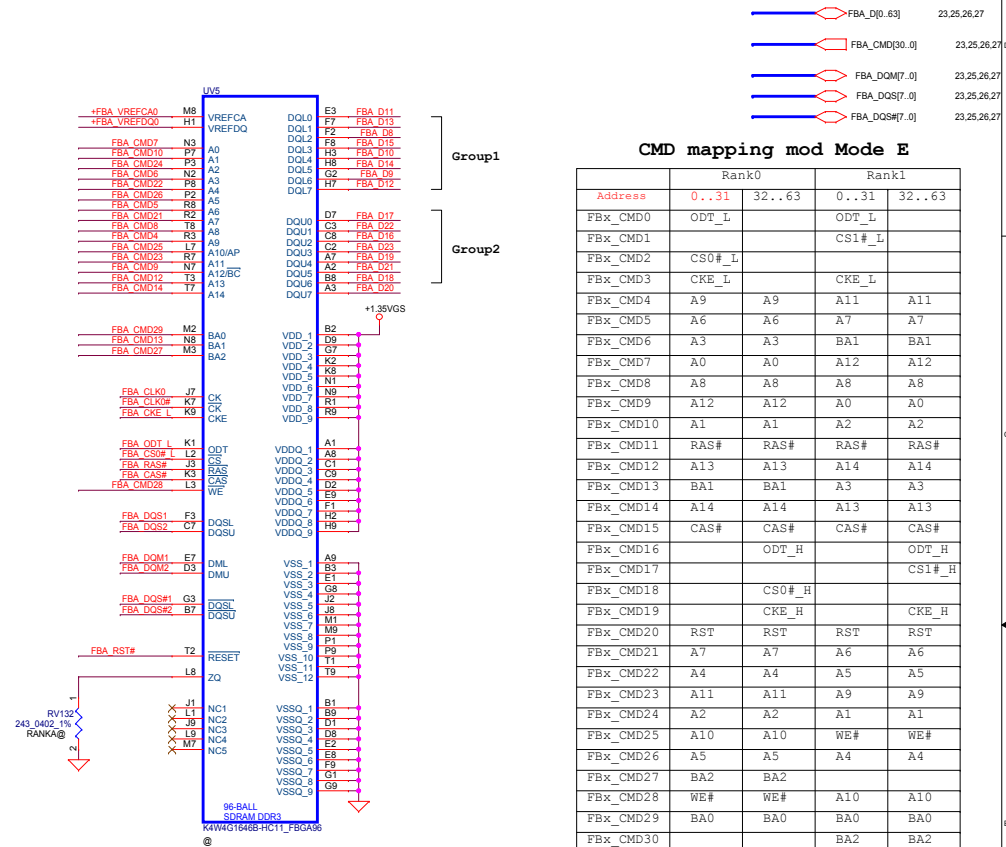
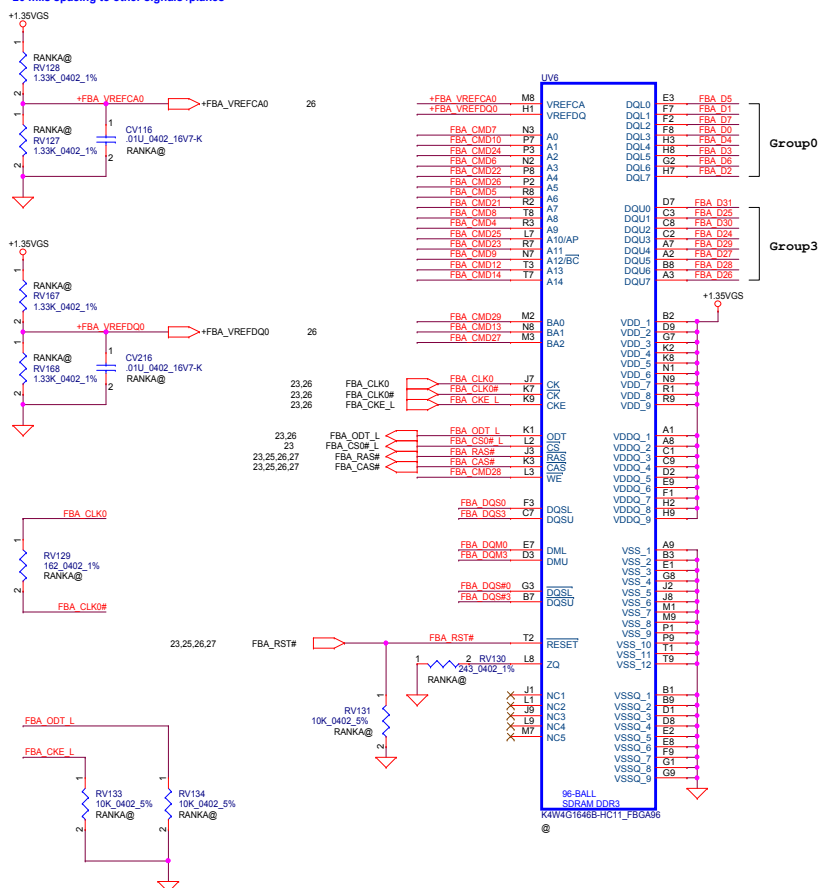
CALIBRATION PIN

CALIBRATION PIN	DDR3
FB_CAL x PD_VDDQ	40.2ohm
FB_CAL x PU_GND	42.2ohm
FB_CAL x TERM_GND	51.1ohm

+1.35V TO +1.35VGS







UVS SIDE

+1.35VGS

0.1U_0402_1007K C129

1 2

1 2

1U_0603_25V6M C130

1 2

1 2

1U_0603_25V6M C131

1 2

1 2

1U_0603_25V6M C132

1 2

1 2

1U_0603_25V6M C133

1 2

1 2

RANKA@ CD@ RANKA@ RANKA@ RANKA@

For RF

+1.35VGS

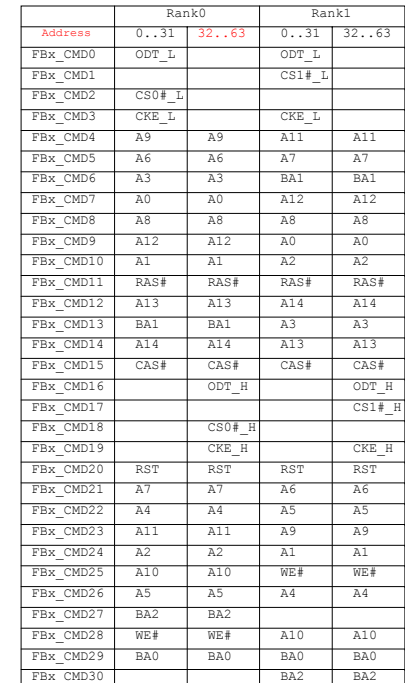
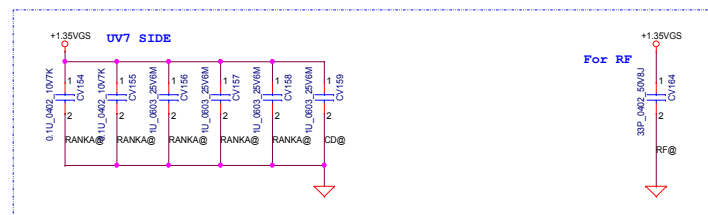
33P_0402_50V6L C139

1 2

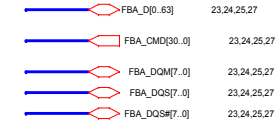
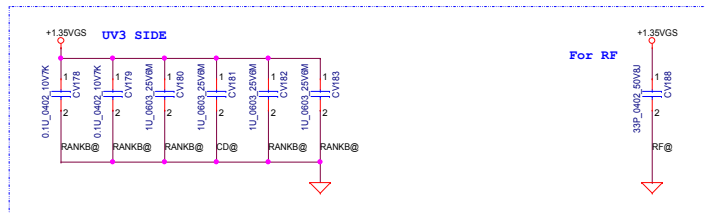
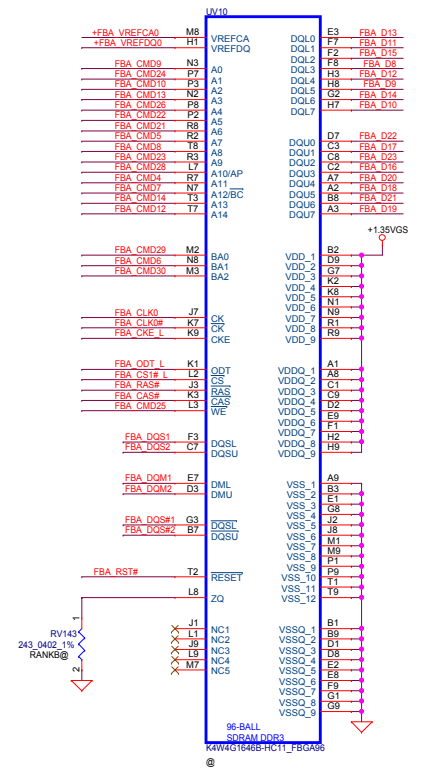
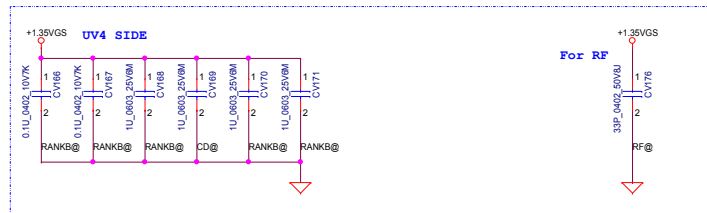
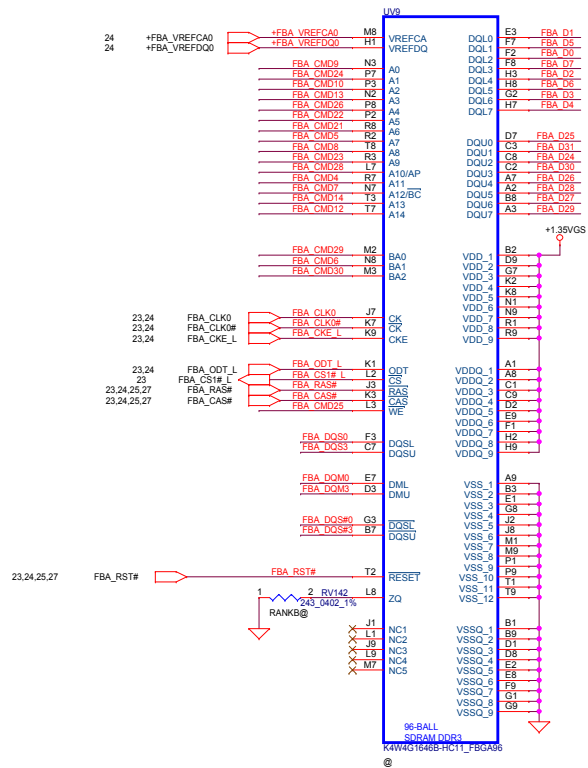
1 2

RF@

The diagram shows two circuit sections. The first section, labeled "UV8 SIDE", is a ladder network with a +1.35VGS supply at the top. It consists of a series of capacitors and inductors: a 11U_0402_1007K capacitor (Cv142) in series with a 11U_0402_1007K capacitor (Cv143) in parallel with a 11U_0603_25V0M inductor (Cv144). This is followed by a 11U_0603_25V0M inductor (Cv145) in series with a 11U_0603_25V0M inductor (Cv146) in parallel with a 11U_0603_25V0M inductor (Cv147). The output is labeled "RANKA@". The second section, labeled "For RF", shows a +1.35VGS supply connected to a 33P_0402_500RJ capacitor (Cv152) in series with the output labeled "RF@".



at least 16 mils width(optimal)
20 mils spacing to other signals /planes

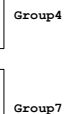


Group1
Group2

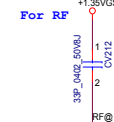
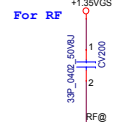
CMD mapping mod Mode E

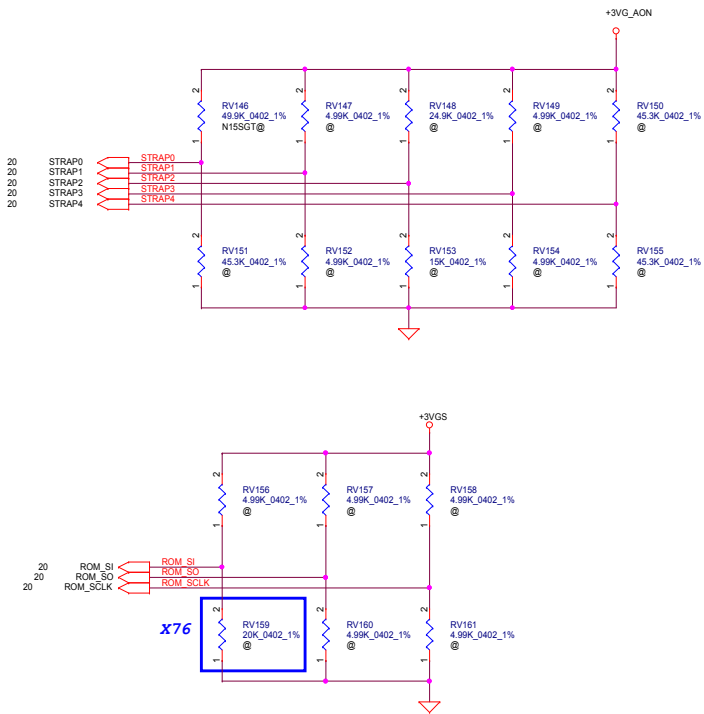
Address	Rank0		Rank1	
	0..31	32..63	0..31	32..63
FbX_CMD0	ODT_L		ODT_L	
FbX_CMD1			CS1#_L	
FbX_CMD2	CS0#_L			
FbX_CMD3	CKE_L		CKE_L	
FbX_CMD4	A9	A9	A11	A11
FbX_CMD5	A6	A6	A7	A7
FbX_CMD6	A3	A3	BA1	BA1
FbX_CMD7	A0	A0	A12	A12
FbX_CMD8	A8	A8	A8	A8
FbX_CMD9	A12	A12	A0	A0
FbX_CMD10	A1	A1	A2	A2
FbX_CMD11	RAS#	RAS#	RAS#	RAS#
FbX_CMD12	A13	A13	A14	A14
FbX_CMD13	BA1	BA1	A3	A3
FbX_CMD14	A14	A14	A13	A13
FbX_CMD15	CAS#	CAS#	CAS#	CAS#
FbX_CMD16		ODT_H		CS1#_H
FbX_CMD17				
FbX_CMD18		CS0#_H		
FbX_CMD19		CKE_H		CKE_H
FbX_CMD20	RST	RST	RST	RST
FbX_CMD21	A7	A7	A6	A6
FbX_CMD22	A4	A4	A5	A5
FbX_CMD23	A11	A11	A9	A9
FbX_CMD24	A2	A2	A1	A1
FbX_CMD25	A10	A10	WE#	WE#
FbX_CMD26	A5	A5	A4	A4
FbX_CMD27	BA2	BA2		
FbX_CMD28	WE#	WE#	A10	A10
FbX_CMD29	BA0	BA0	BA0	BA0
FbX_CMD30			BA2	BA2

at least 16 mils width(optimal)
20 mils spacing to other signals /planes



	Rank0		Rank1	
Address	0..31	32..63	0..31	32..63
FBx_CMD0	ODT_L		ODT_L	
FBx_CMD1			CS1#_L	
FBx_CMD2	CS0#_L			
FBx_CMD3	CKE_L		CKE_L	
FBx_CMD4	A9	A9	A11	A11
FBx_CMD5	A6	A6	A7	A7
FBx_CMD6	A3	A3	BA1	BA1
FBx_CMD7	A0	A0	A12	A12
FBx_CMD8	A8	A8	A8	A8
FBx_CMD9	A12	A12	A0	A0
FBx_CMD10	A1	A1	A2	A2
FBx_CMD11	RAS#	RAS#	RAS#	RAS#
FBx_CMD12	A13	A13	A14	A14
FBx_CMD13	BA1	BA1	A3	A3
FBx_CMD14	A14	A14	A13	A13
FBx_CMD15	CAS#	CAS#	CAS#	CAS#
FBx_CMD16		ODT_H		ODT_H
FBx_CMD17				CS1#_H
FBx_CMD18		CS0#_H		
FBx_CMD19		CKE_H		CKE_H
FBx_CMD20	RST	RST	RST	RST
FBx_CMD21	A7	A7	A6	A6
FBx_CMD22	A4	A4	A5	A5
FBx_CMD23	A11	A11	A9	A9
FBx_CMD24	A2	A2	A1	A1
FBx_CMD25	A10	A10	WE#	WE#
FBx_CMD26	A5	A5	A4	A4
FBx_CMD27	BA2	BA2		
FBx_CMD28	WE#	WE#	A10	A10
FBx_CMD29	BA0	BA0	BA0	BA0
FBx_CMD30			BA2	BA2





Physical Strapping pin	Power Rail	Logical Strapping Bit3	Logical Strapping Bit2	Logical Strapping Bit1	Logical Strapping Bit0
ROM_SCLK	+3VGS	SOR3_EXPOSED	SOR2_EXPOSED	SOR1_EXPOSED	SOR0_EXPOSED
ROM_SI	+3VGS	RAM_CFG[3]	RAM_CFG[2]	RAM_CFG[1]	RAM_CFG[0]
ROM_SO	+3VGS	DEVID_SEL	PCIE_CFG	SMB_ALT_ADDR	VGA_DEVICE
STRAP0	+3VGS	Reserved(keep pull-up and pull-down footprint and stuff 50Kohm pull-up)			
STRAP1	+3VGS	Reserved(keep pull-up and pull-down footprint and not stuff by default)			
STRAP2	+3VGS				
STRAP3	+3VGS				
STRAP4	+3VGS				

Resistor Values	Pull-up to +3VGS	Pull-down to Gnd
4.99K	1000	0000
10K	1001	0001
15K	1010	0010
20K	1011	0011
24.9K	1100	0100
30.1K	1101	0101
34.8K	1110	0110
45.3K	1111	0111

Physical Strapping pin	Power Rail	Strap Mapping
ROM_SCLK	+3VGS	SMB_ALT_ADDR
ROM_SI	+3VGS	SUB_VENDOR
ROM_SO	+3VGS	VGA_DEVICE
STRAP0	+3VGS	RAM_CFG[0]
STRAP1	+3VGS	RAM_CFG[1]
STRAP2	+3VGS	RAM_CFG[2]
STRAP3	+3VGS	RAM_CFG[3]
STRAP4	+3VGS	PCIE_MAX_SPEED

DEVID_SEL	
0	(Default)
1	

PCIE_CFG	
0	(Default)
1	

SMBUS_ALT_ADDR	
0	0x9E (Default)
1	0x9C (Multi-GPU usage)


VGA_DEVICE	
0	3D Device (Class Code 302h)
1	VGA Device (Default)


GPU	FB Memory (DDR3)	ROM_SI	ROM_SO	ROM_SCLK	STRAP0	STRAP1	STRAP2	STRAP3	STRAP4
N15S-GT	H5TC4G63AFR-11C	0x3	PD 4.99K	PD 4.99K	PU 49.9K	Un-stuff	Un-stuff	Un-stuff	Un-stuff
	256M x 16	PD 20K							
	MT41J256M16HA-093G:E	0x4							
	256M x 16	PD 24.9K							
	K4W4G1646D-BC1A	0x5							
	256M x 16	PD 30.1K							

GPU	FB Memory (DDR3)	STRAP3	STRAP2	STRAP1	STRAP0	STRAP4	ROM_SI	ROM_SO	ROM_SCLK
N15V-GM	H5TC4G63AFR-11C	PD 10K	PU 10K	PD 10K	PD 10K	PD 10K	PD 10K	PD 10K	PD 10K
	256M x 16	0x4							
	MT41J256M16HA-093G:E	PU 10K	PU 10K	PD 10K	PU 10K				
	256M x 16	0xD							
	K4W4G1646D-BC1A	PU 10K	PD 10K	PD 10K	PU 10K				
	256M x 16	0x9							

VRAM	X76	VRAM P/N
Samsung	X76409JVL01	SA00005SH10
	X76409JVL51 (1G 32Mx16)	
Micron	X76409JVL02	SA00005M100
	X76409JVL02 (2G 64Mx32)	
Hynix		


需要修改，Table為G15料號

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				Date: Wednesday, July 16, 2014	Sheet 29 of 60	

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		Security Classification		LC Future Center Secret Data		Title			
		Issued Date		2014/06/28		Deciphered Date			
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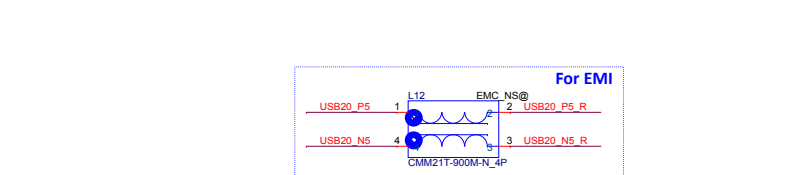
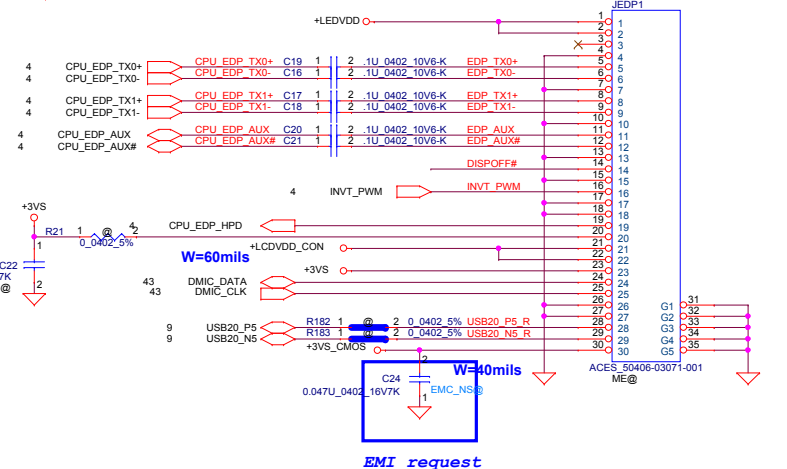
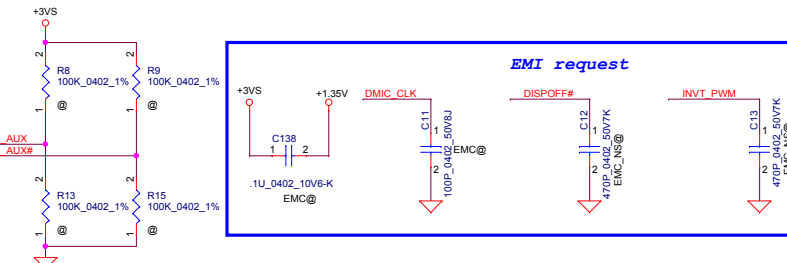
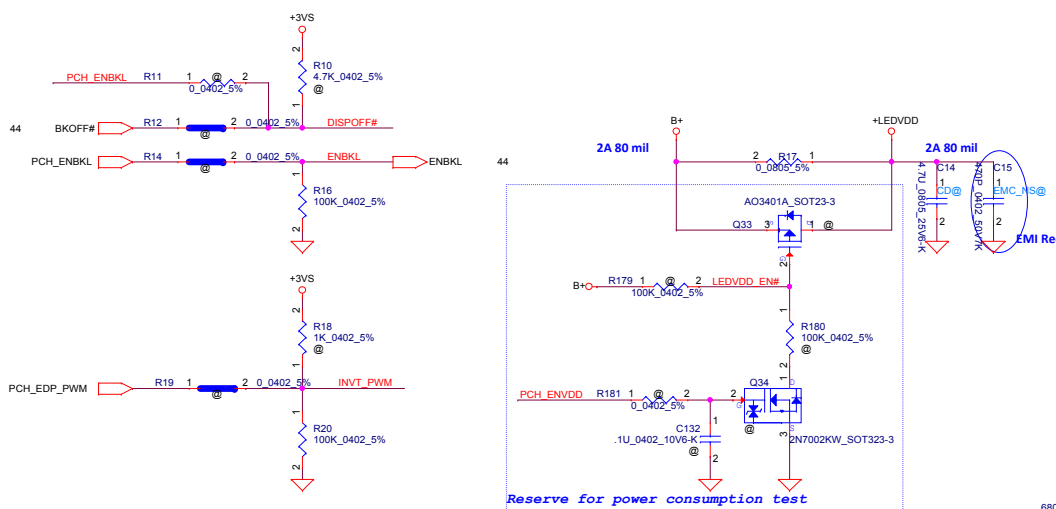
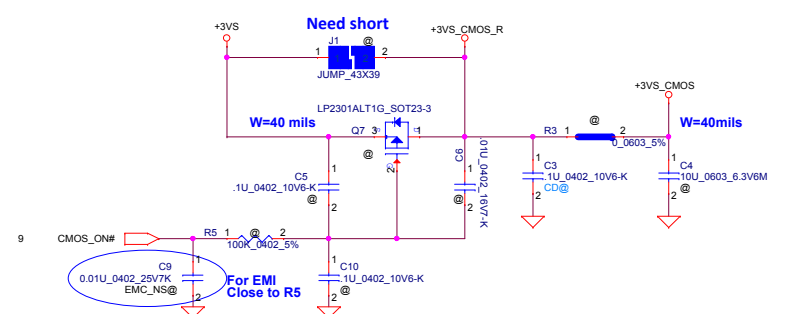
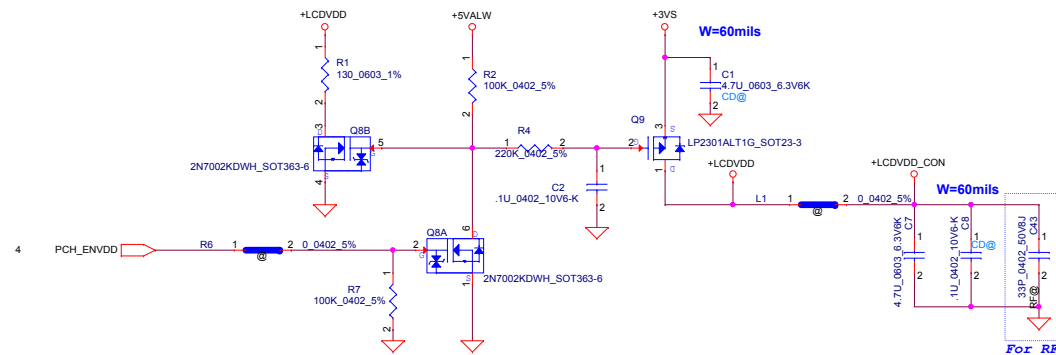
5	4	3	2	1					
D				D					
C				C					
B				B					
A				A					
		Security Classification		LC Future Center Secret Data		Title			
		Issued Date		2014/06/28		Deciphered Date		2015/06/28	
		THIS SHEET OF ENGINEERING DRAWING IS THE PROPRIETARY PROPERTY OF LC FUTURE CENTER AND CONTAINS CONFIDENTIAL AND TRADE SECRET INFORMATION. THIS SHEET MAY NOT BE TRANSFERRED FROM THE CUSTODY OF THE COMPETENT DIVISION OF R&D DEPARTMENT EXCEPT AS AUTHORIZED BY LC FUTURE CENTER NEITHER THIS SHEET NOR THE INFORMATION IT CONTAINS MAY BE USED BY OR DISCLOSED TO ANY THIRD PARTY WITHOUT PRIOR WRITTEN CONSENT OF LC FUTURE CENTER.		Size		Document Number		Rev	
				Custom		BILG1/AILG1/AILZ1		0.4	
				Date:		Wednesday, July 16, 2014		Sheet 31 of 60	
5	4	3	2	1					

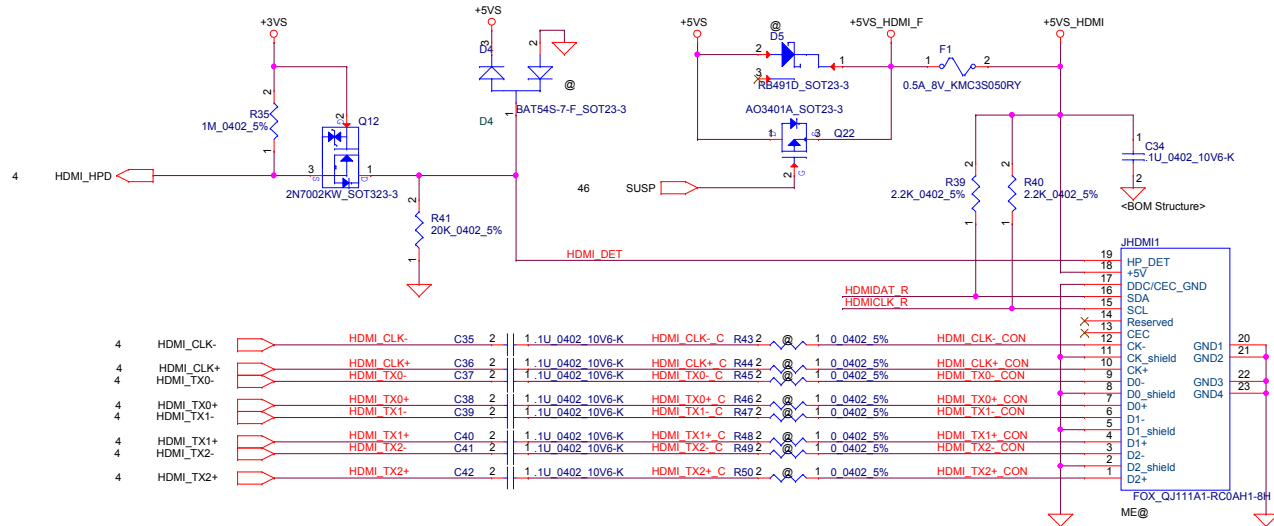
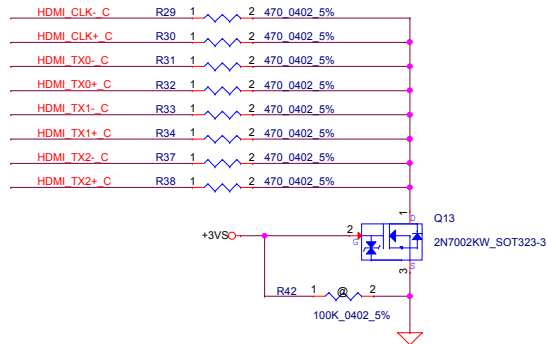
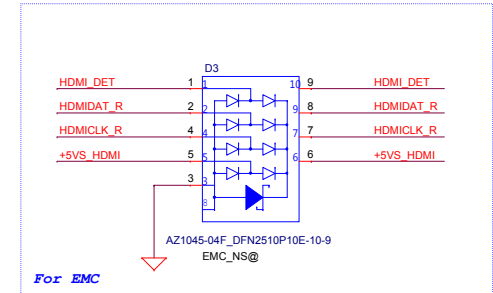
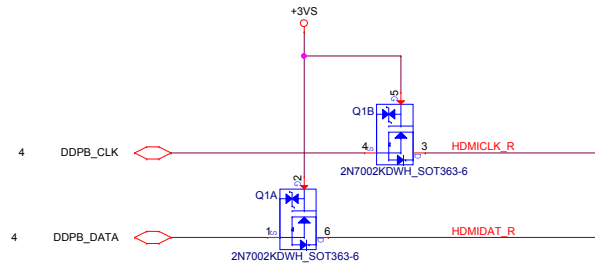
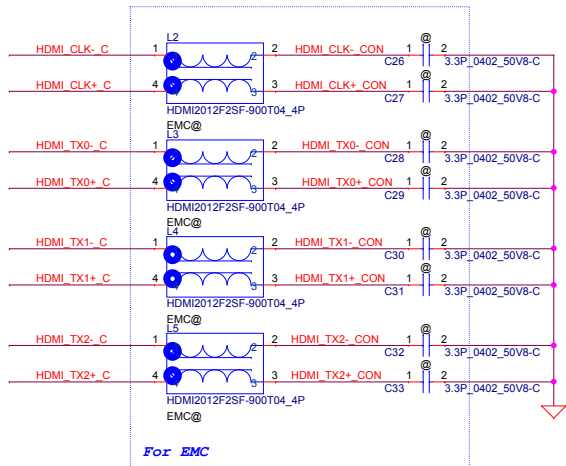


Security Classification		LC Future Center Secret Data		Title			
Issued Date	2014/06/28	Deciphered Date	2015/06/28	Blank			
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				Custom	BIIG1/AIIG1/AIILZ1		0.4
				Date:	Wednesday, July 16, 2014		
3		2		1		Sheet 32 of 60	

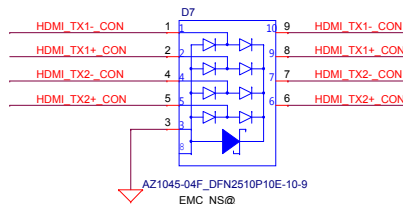
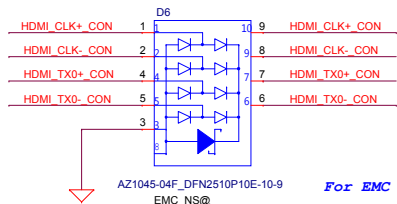
LCD POWER CIRCUIT


CMOS Camera

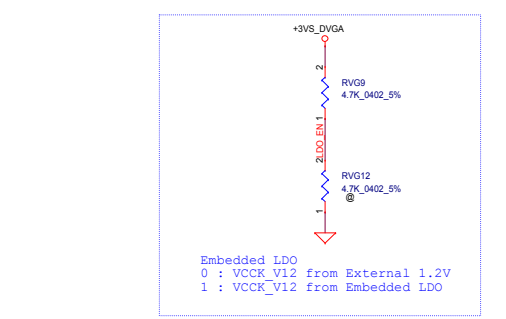
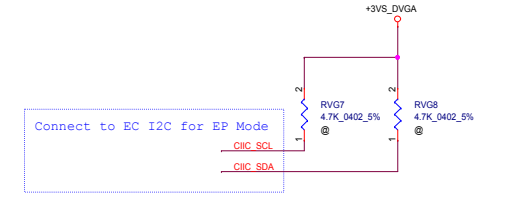
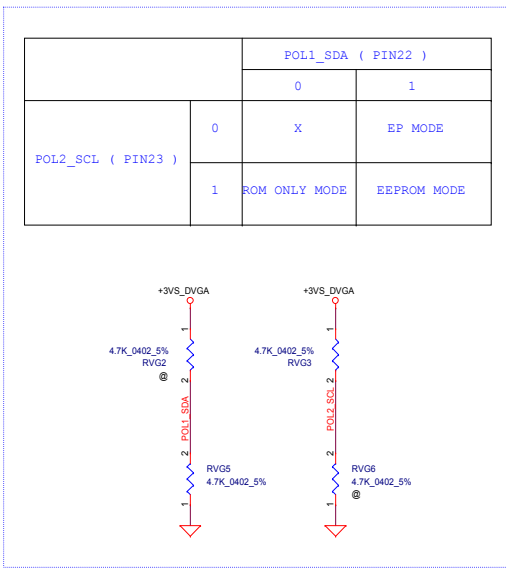
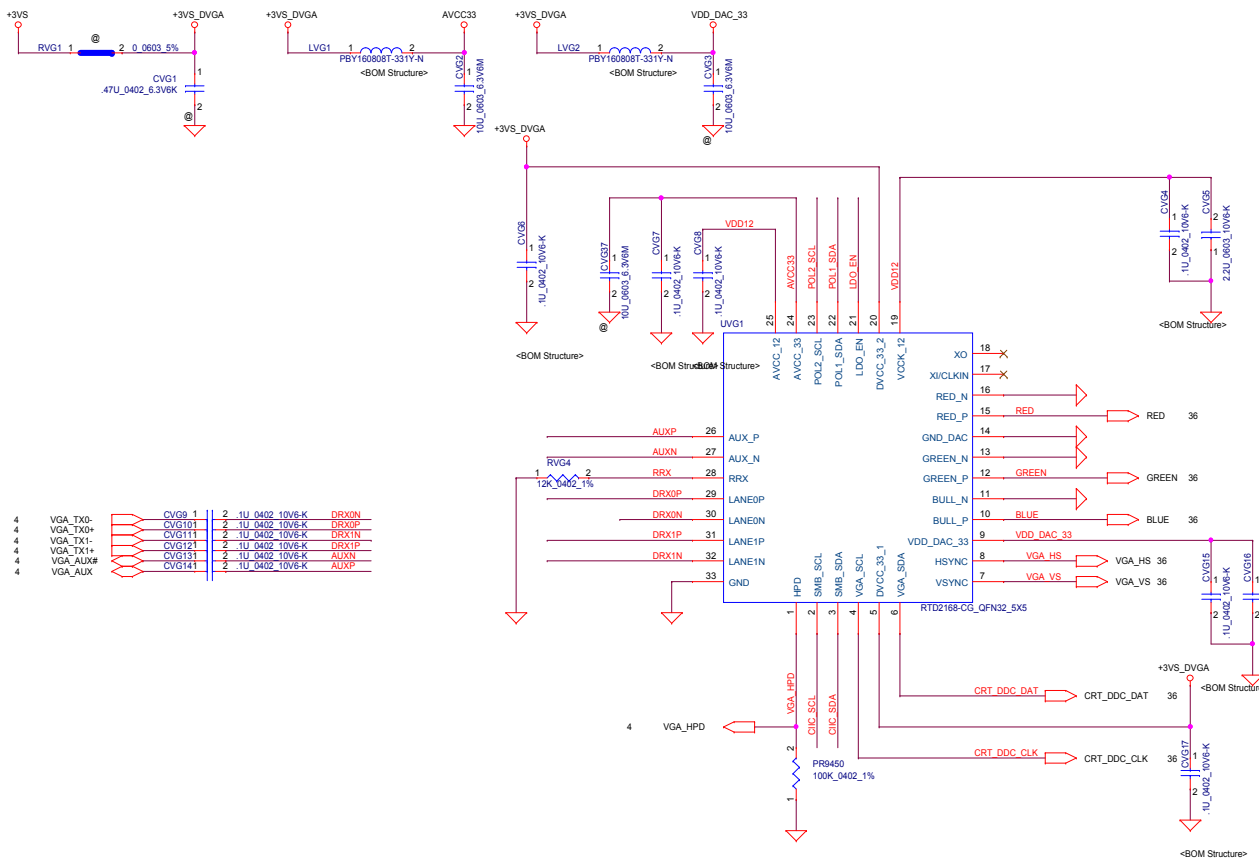




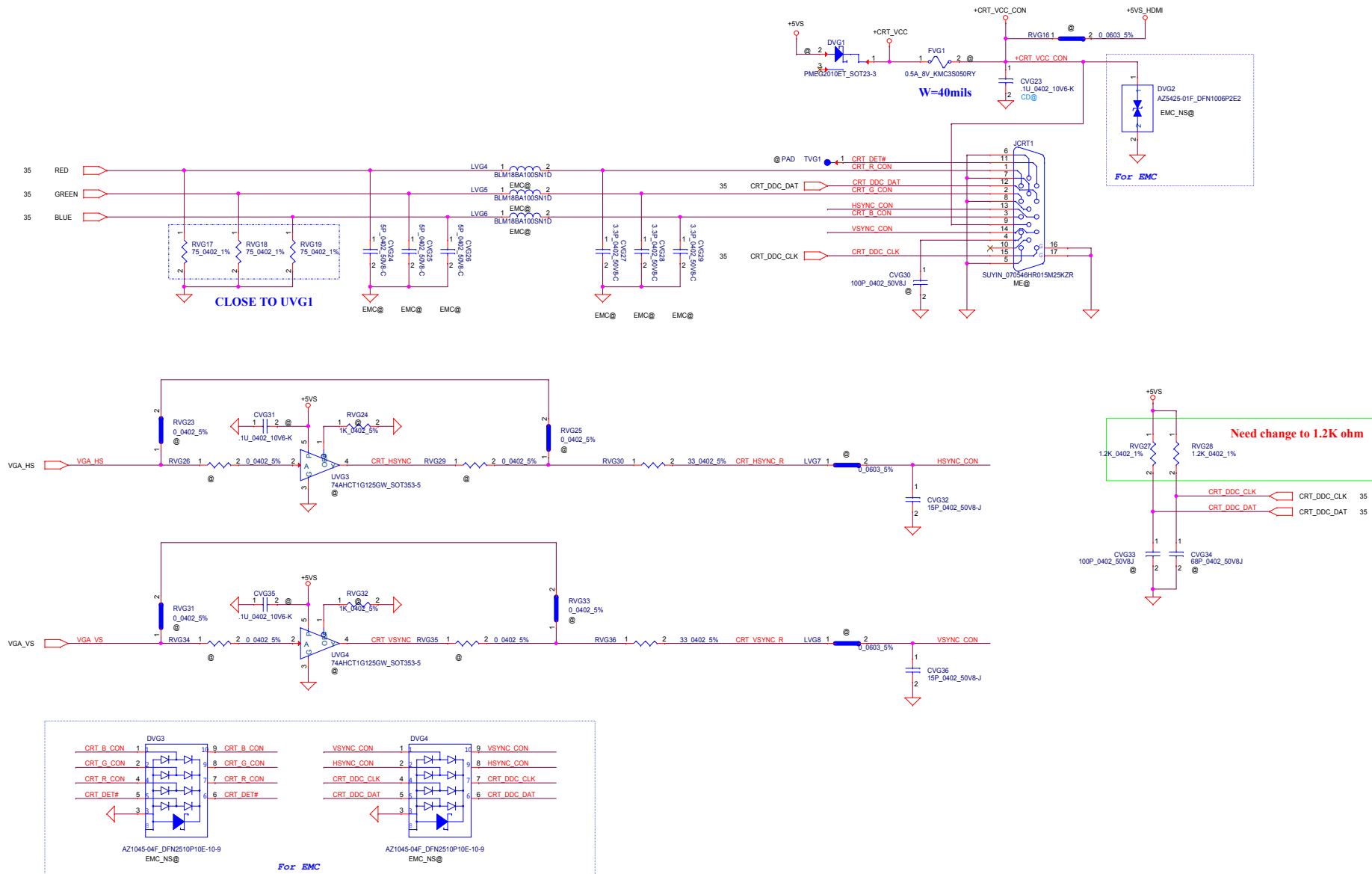
Close to JHDMI1



Security Classification		LC Future Center Secret Data		Title		
Issued Date	2014/06/28	Deciphered Date	2015/06/28	HDMI_CONN		
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DEPARTMENT EXCEPT AS AUTHORIZED BY LC FUTURE CENTER. NEITHER THIS SHEET NOR THE INFORMATION IT CONTAINS MAY BE USED BY OR DISCLOSED TO ANY THIRD PARTY WITHOUT PRIOR WRITTEN CONSENT OF LC FUTURE CENTER.				Custom	BILG1/AILG1/AILZ1	
				Date:	Wednesday, July 16, 2014	Sheet 34 of 60



CRT Connector



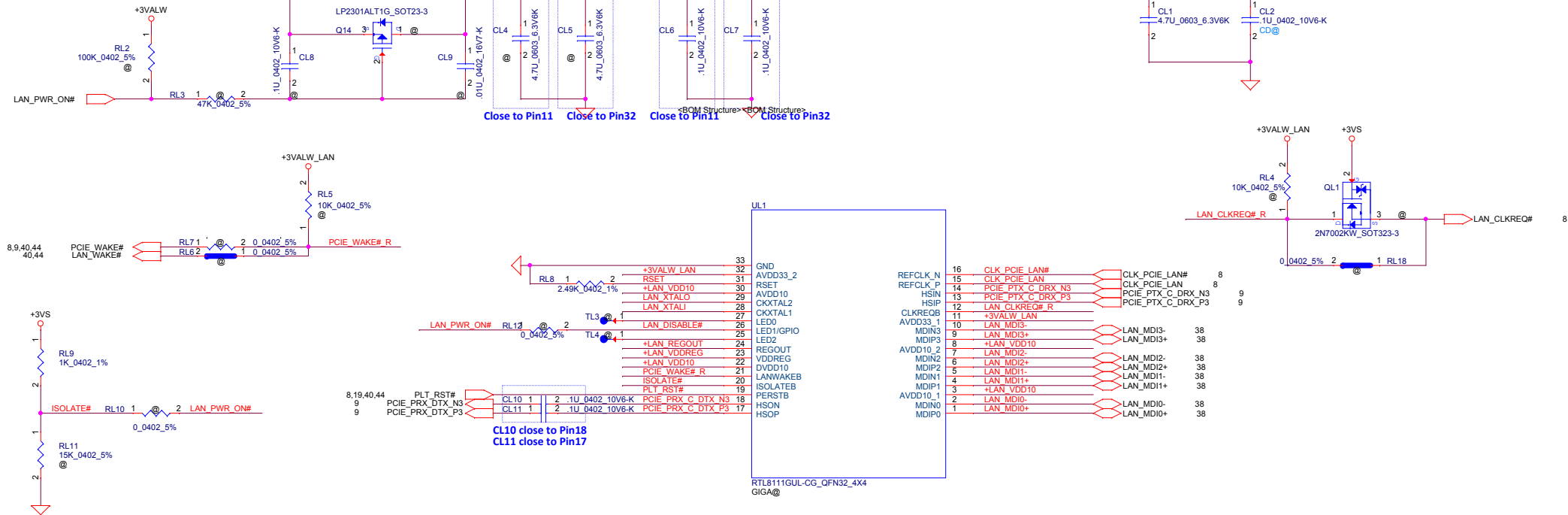
+3VALW TO +3VALW_LAN

+3VALW_LAN rising time (10%~90%):
0.5ms<spec<100ms

Need short

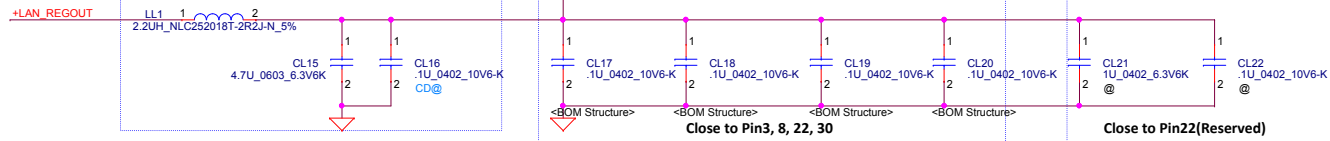
width : 40 mils

Close to Pin11 Close to Pin32 Close to Pin11 Close to Pin32



CL10 close to Pin18
CL11 close to Pin17

For RTL8111GUL/RTL8106EUL (SWR mode)

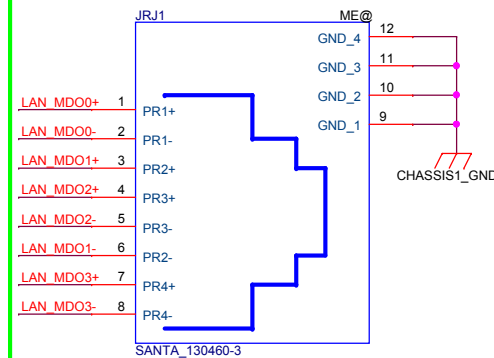
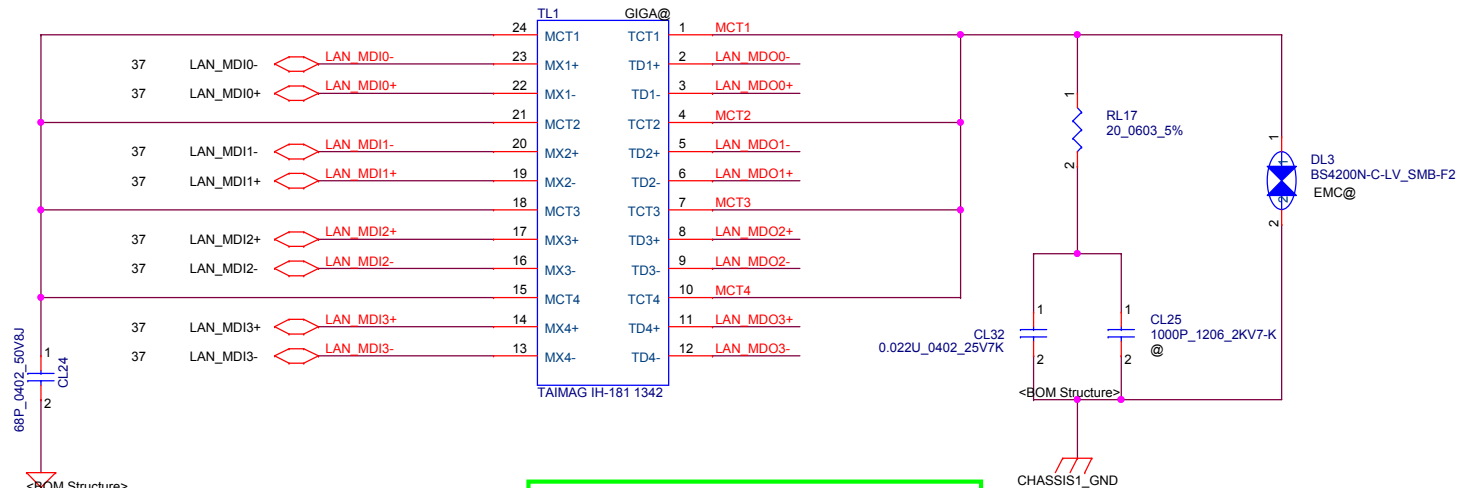
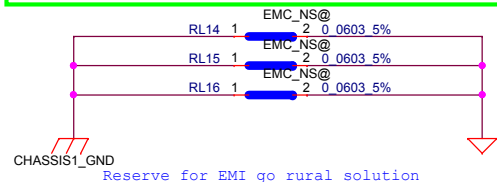
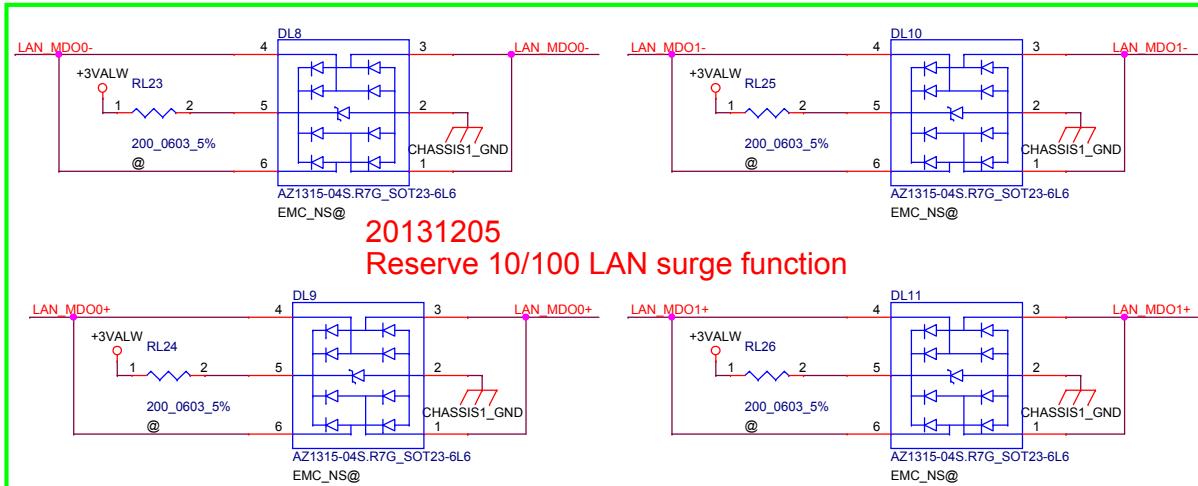
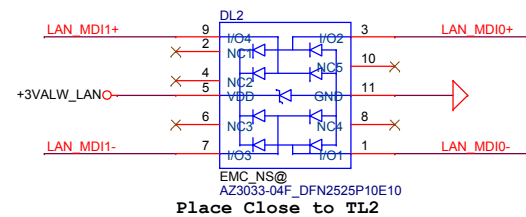
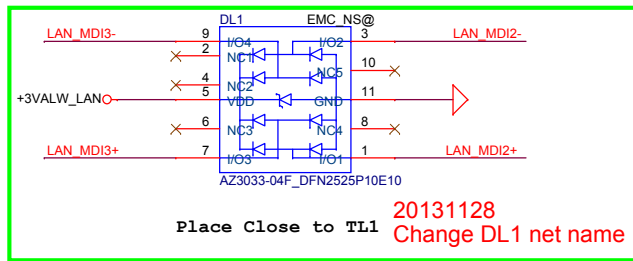


Layout Note: LL1 must be within 200mil to Pin36,
CL15, CL16 must be within 200mil to LL1
+LAN_REGOUT: Width =60mil

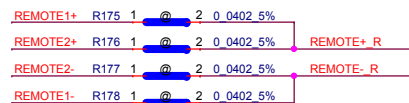
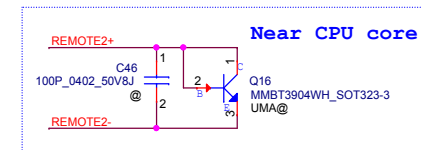
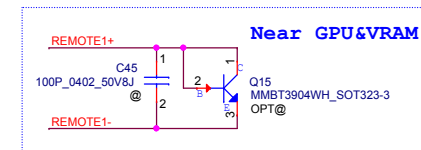
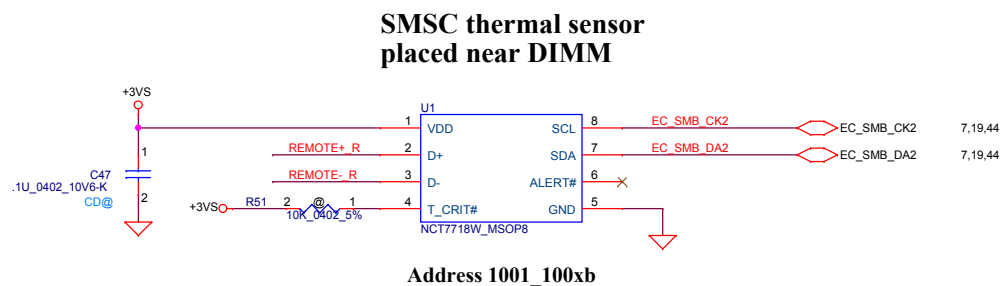
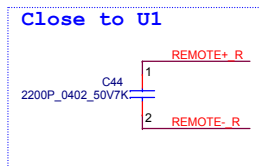
Security Classification		LC Future Center Secret Data		Title	
Issued Date	2014/06/28	Deciphered Date	2015/06/28	LAN_RTL8111GUL/RTL8106EUL	
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				Document Number	
				BILG1/AILG1/AILZ1	
Date:		Wednesday, July 16, 2014		Sheet	37 of 60

DL1/DL2
1'S PN:SC300003M00

TL1 GIGA SIVT 璦传

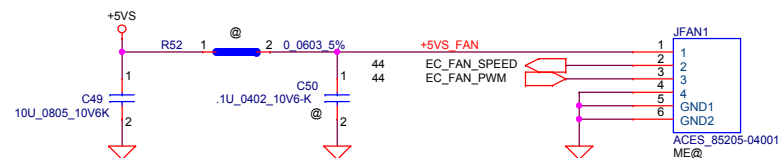


Security Classification		LC Future Center Secret Data		Title	
Issued Date	2014/06/28	Deciphered Date	2015/06/28	LAN_Transformer	
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				B	BILG1/AILG1/AILZ1
				Date:	Friday, July 18, 2014
				Sheet	38 of 60
				Rev	0.4



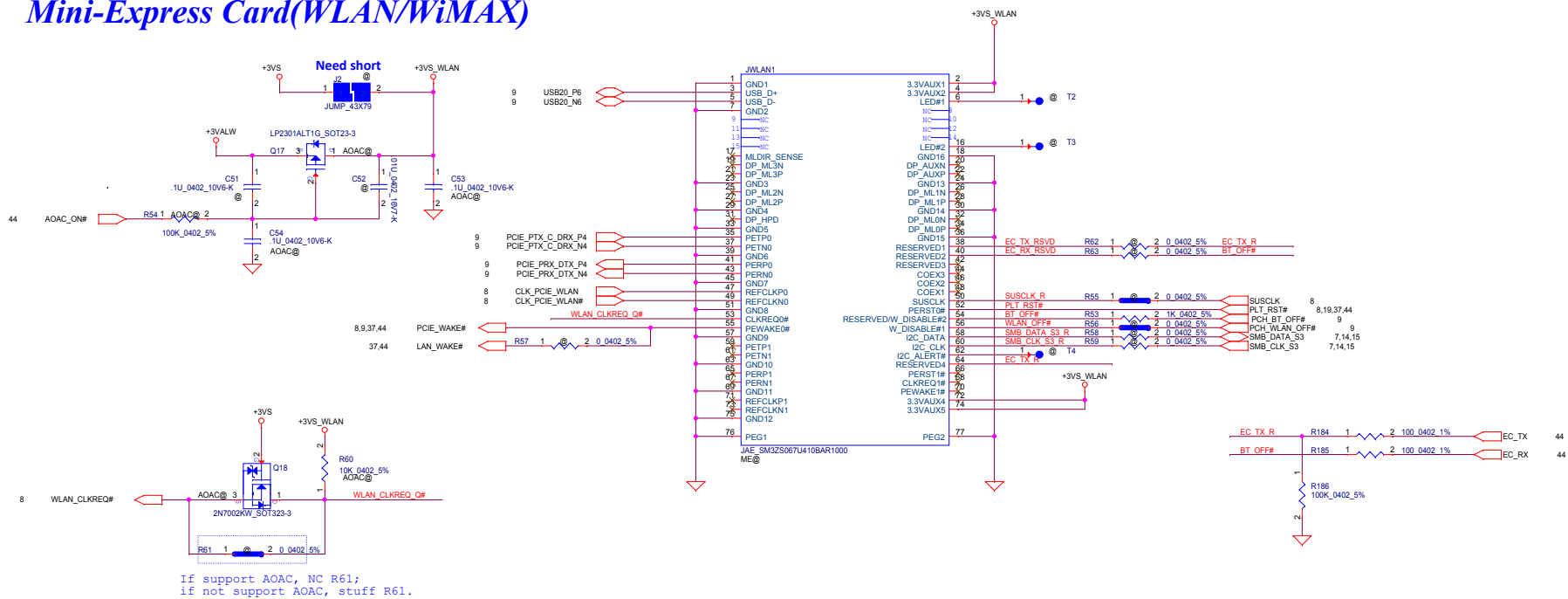
REMOTE+/- R, REMOTE1+/-, REMOTE2+/-:
Trace width/space:10/10 mil
Trace length:<8"


FAN Conn



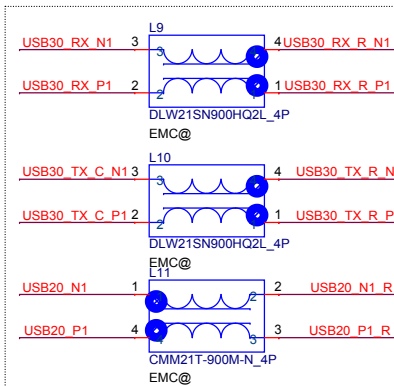
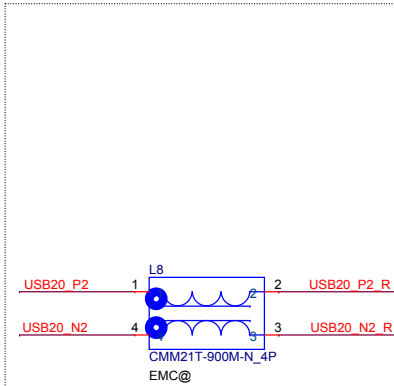
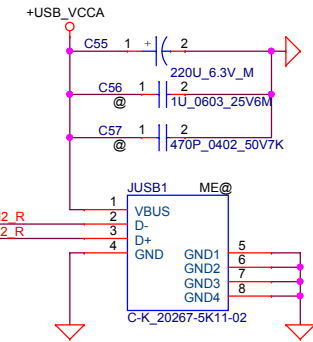
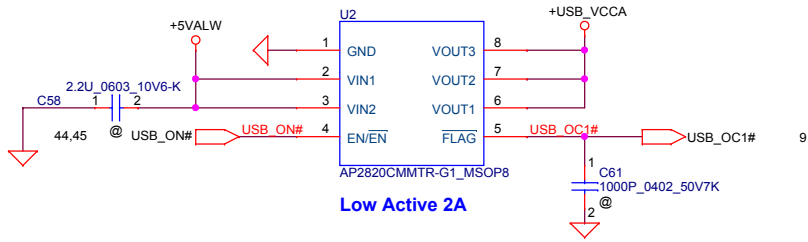
Security Classification		LC Future Center Secret Data		Title	
Issued Date	2014/06/28	Deciphered Date	2015/06/28	Thermal sensor/FAN CONN	
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				Date: Wednesday, July 16, 2014	Rev 0.4
				Sheet 39	of 60

Mini-Express Card(WLAN/WiMAX)

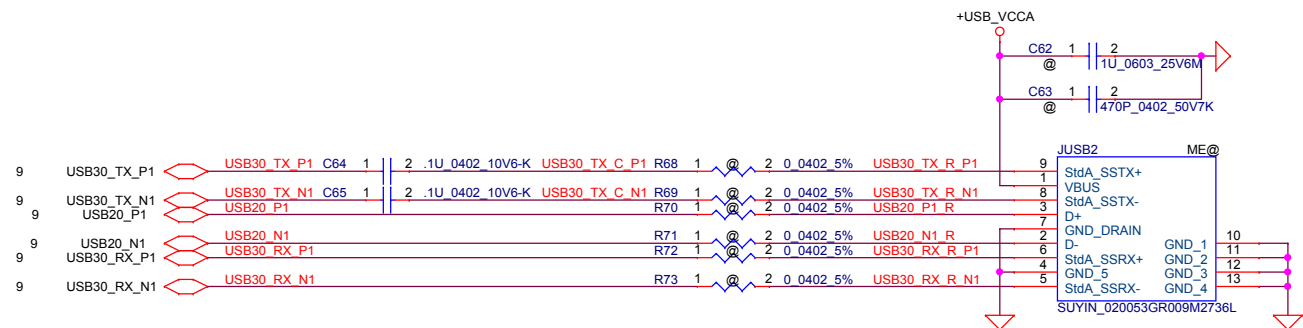
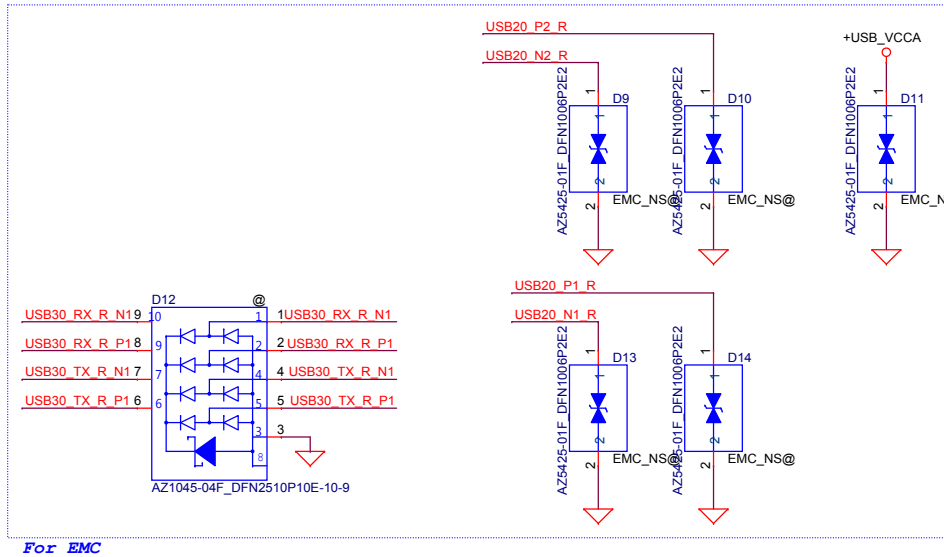



Security Classification		LC FUTURE CENTER Secret Data		Title		
Issued Date	2014/06/28	Deciphered Date	2015/06/28	NGFF WLAN		
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				Date:	Wednesday, July 16, 2014	Sheet 40 of 60

LEFT SIDE USB3.0 PORT X2

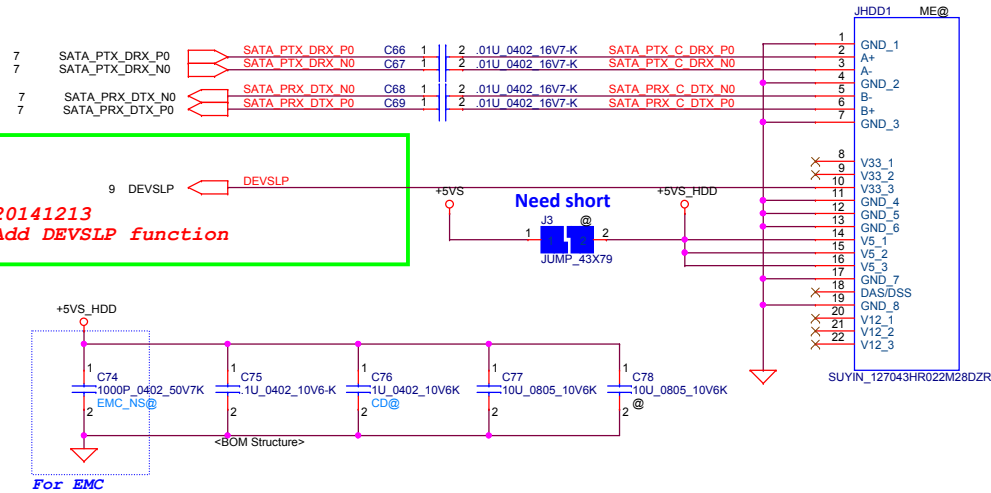


For EMC



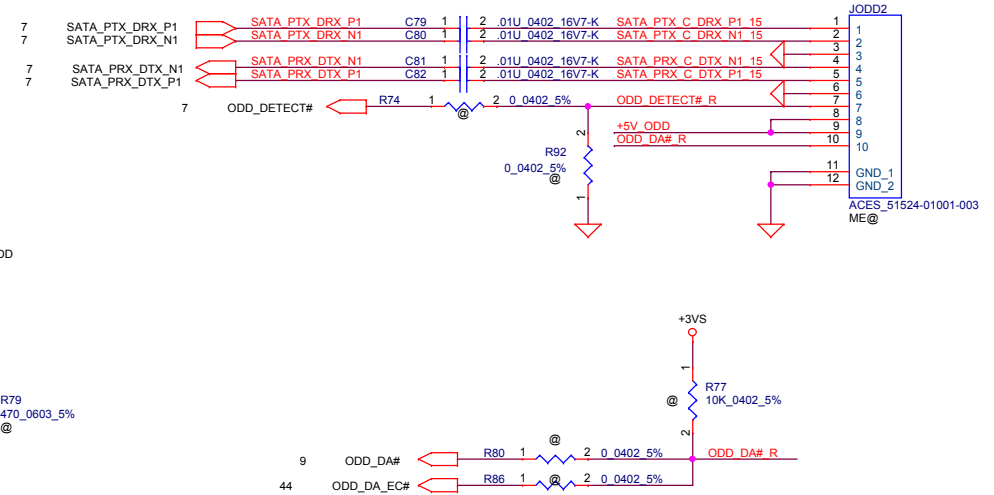
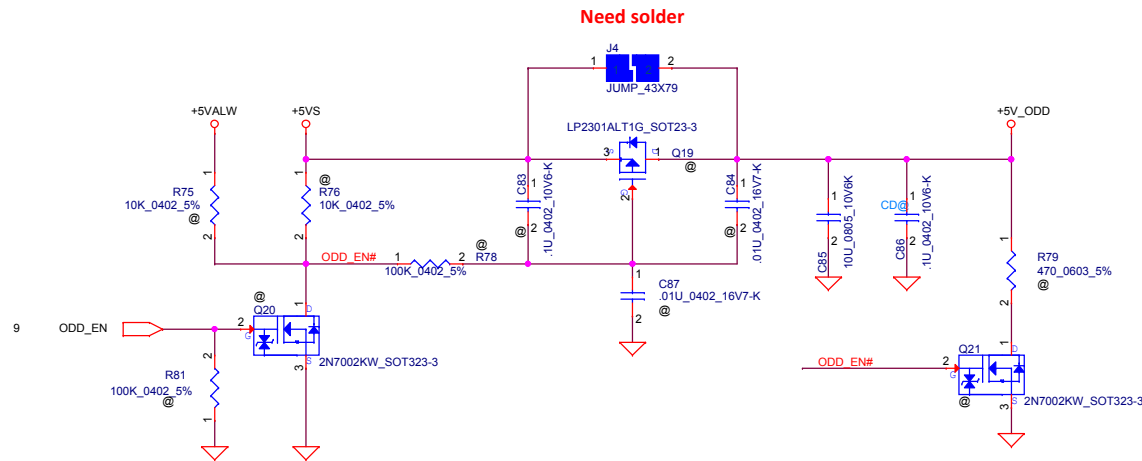
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Issued Date		2014/06/28		Deciphered Date				2015/06/28	
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				Custom		0.4			
				BILG1/AILG1/AILZ1					
Date:		Wednesday, July 16, 2014		Sheet		41 of 60			

SATA HDD Conn.

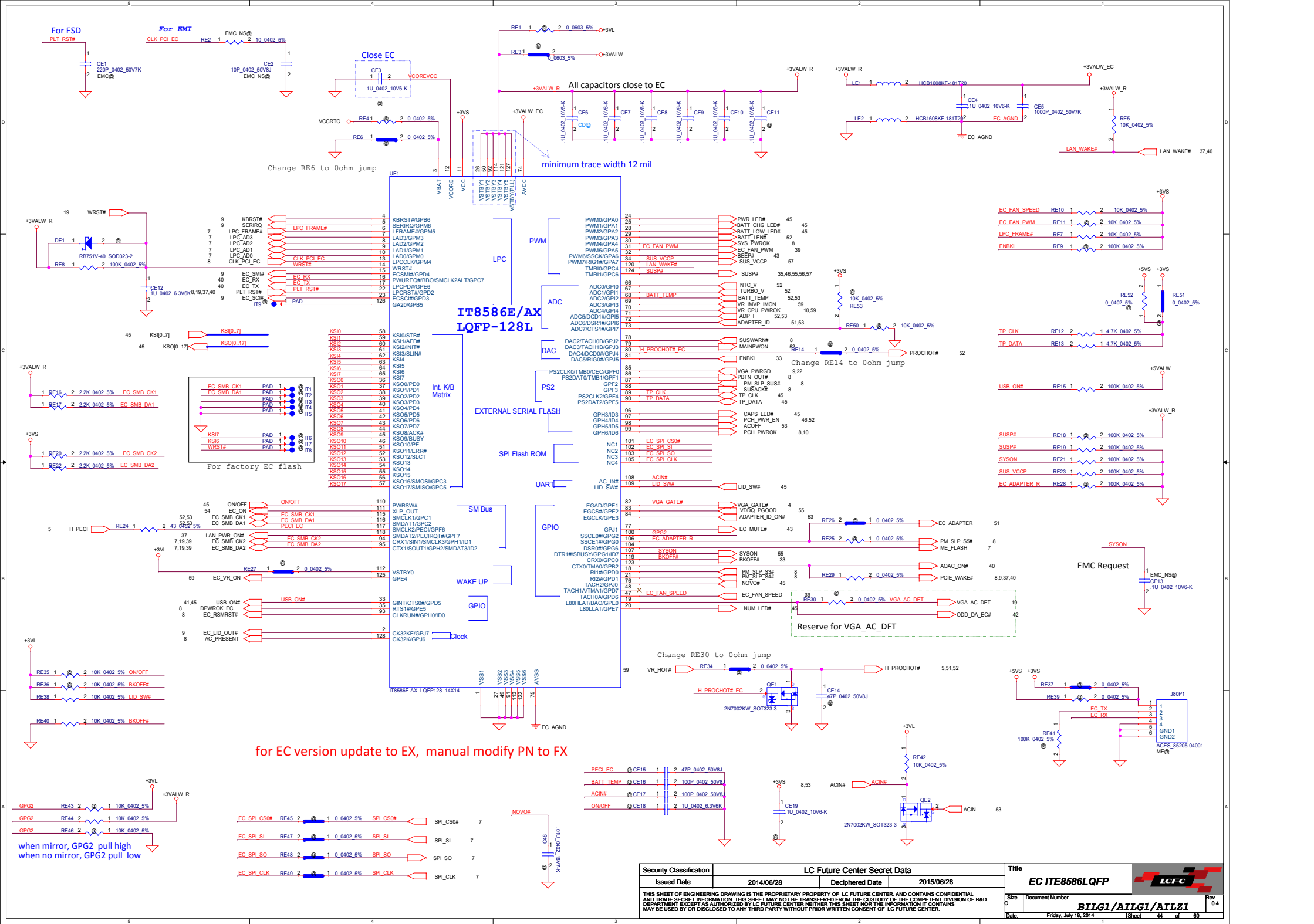


FOR 14"
SATA ODD Conn.

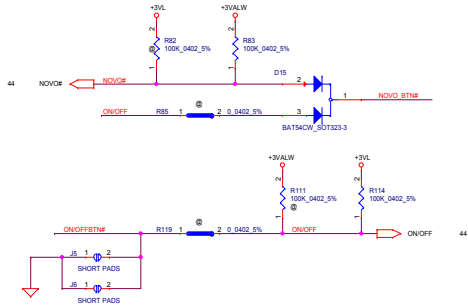
FOR 15"
SATA ODD FFC Conn



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Issued Date	2014/06/28	Deciphered Date	2015/06/28	HDD/ODD CONN	
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				Date Wednesday, July 16, 2014	Rev 0.4
				Sheet 42	of 60

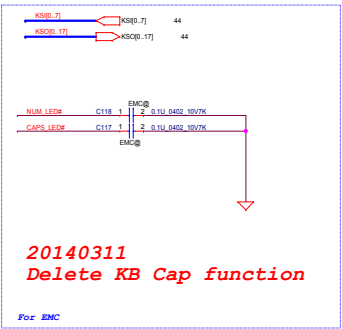


ON/OFF switch



TP/B Connector

K/B Connector

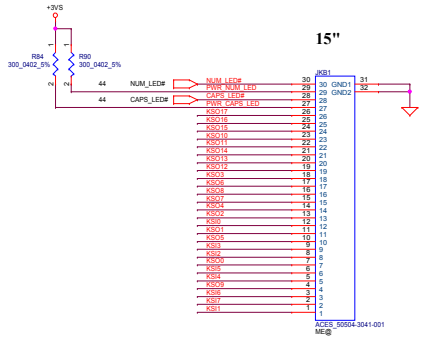


20140311
Delete KB Cap function

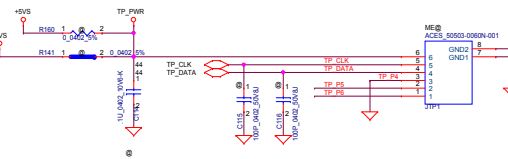
For EMC

20141114
Delete G14 KB function

15"

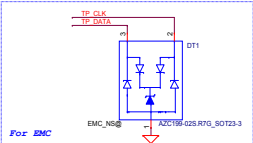


14"	15"
KB_1	KS11_14
KB_2	KS17_14
KB_3	KS16_14
KB_4	KS09_14
KB_5	KS14_14
KB_6	KS15_14
KB_7	KS00_14
KB_8	KS12_14
KB_9	KS13_14
KB_10	KS08_14
KB_11	KS01_14
KB_12	KS10_14
KB_13	KS02_14
KB_14	KS04_14
KB_15	KS07_14
KB_16	KS05_14
KB_17	KS03_14
KB_18	KS06_14
KB_19	KS01_14
KB_20	KS13_14
KB_21	KS14_14
KB_22	KS11_14
KB_23	KS16_14
KB_24	KS15_14

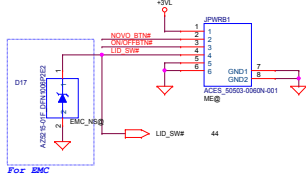


For 14"	For 15"
1 VDD	1 VDD
2 CLK	2 CLK
3 DAT	3 DAT
4 GND	4 GND
5 TP-L	5 TP-L
6 TP-R	6 TP-R

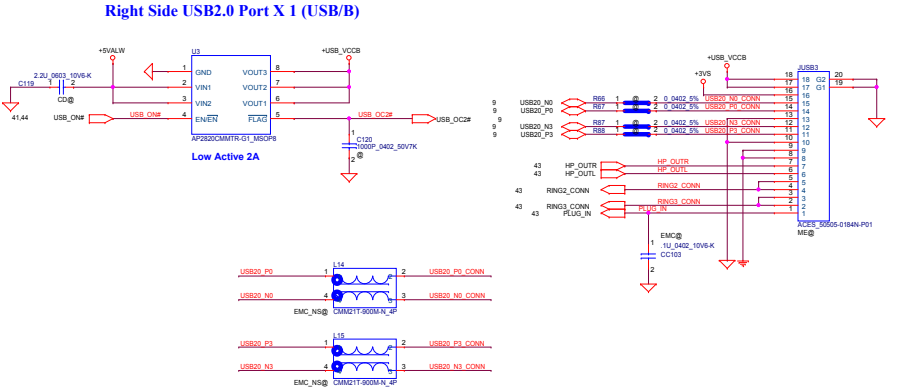
20141114
Delete G14 TP click function



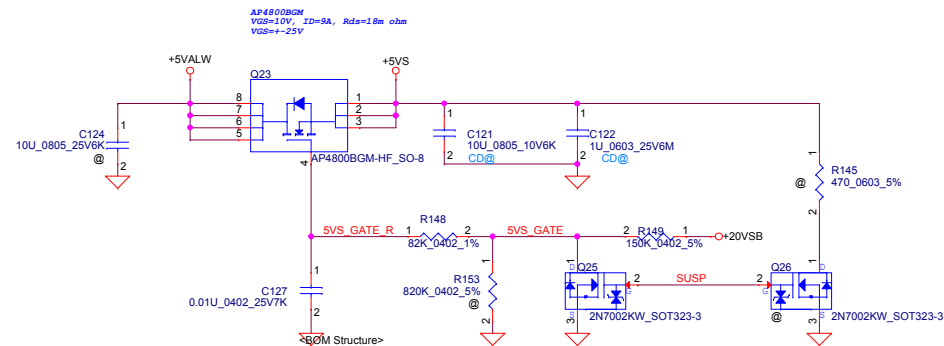
PWR/B Connector



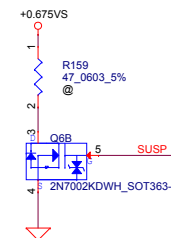
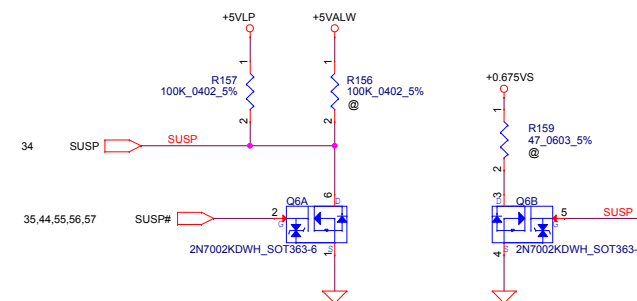
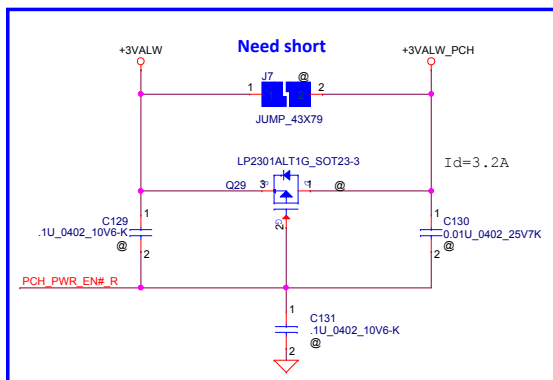
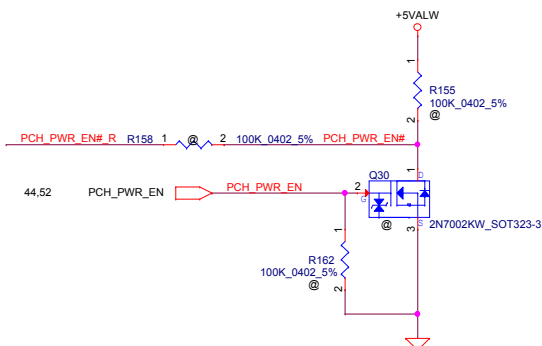
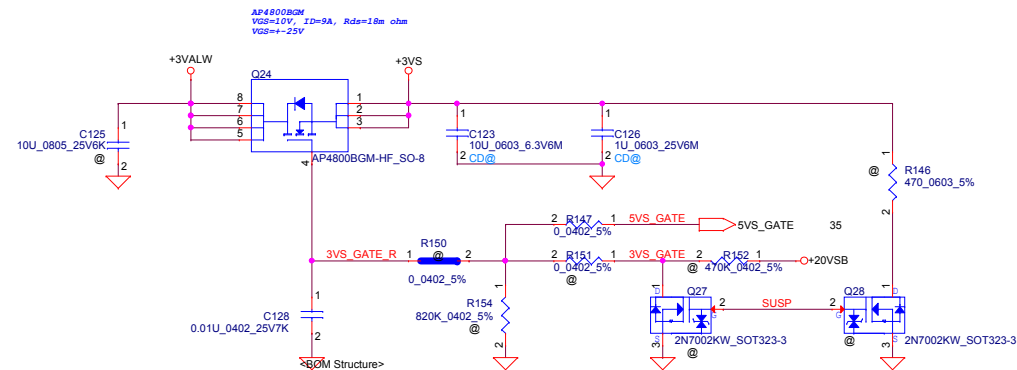
USB I/O Connector

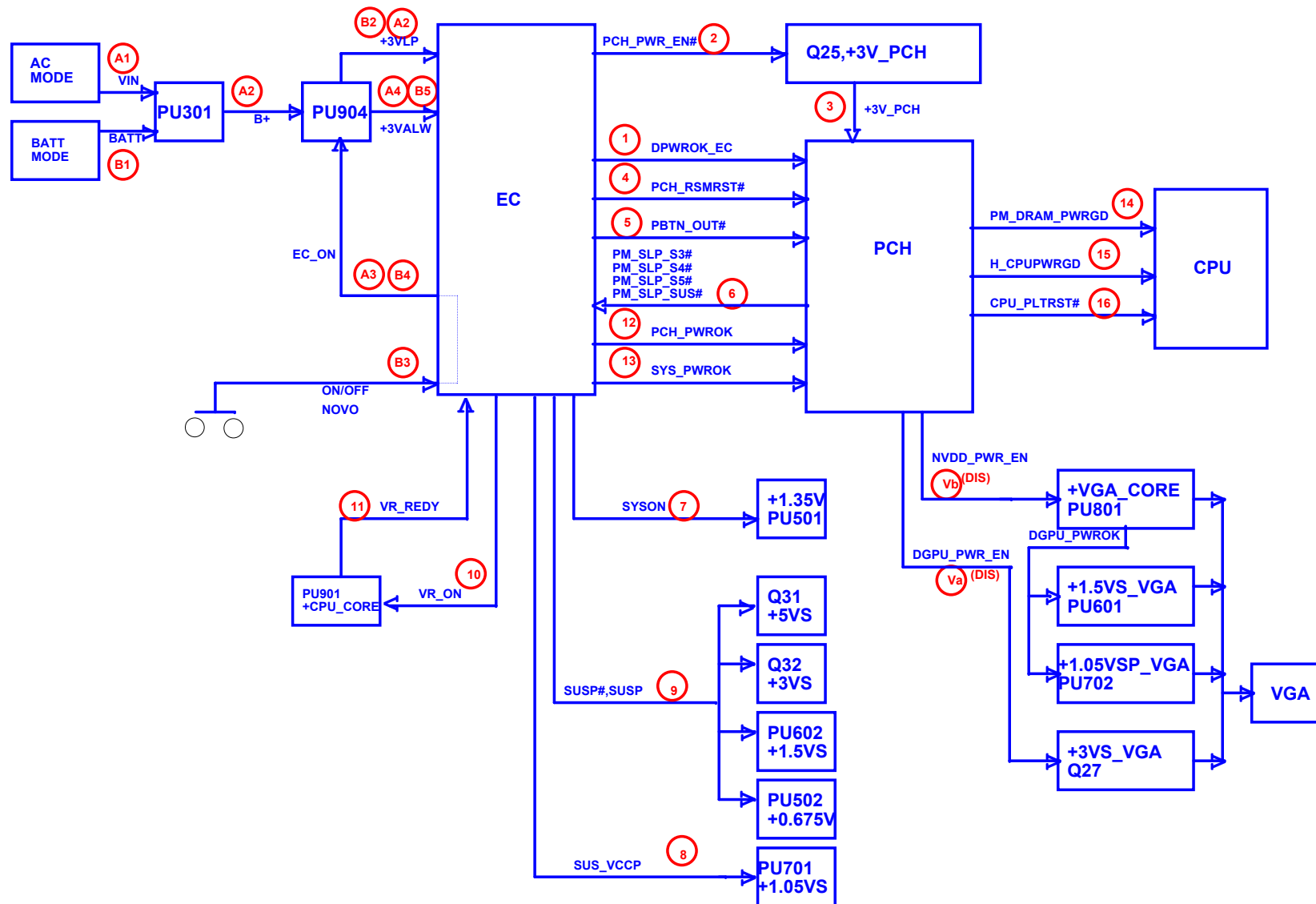


+5VALW to +5VS



+3VALW to +3VS





<

20131203
Delete NH2



pad_c2p3d2p3n



pad_o2p3x2p8d2p3x2p8n

20131203
Change H6 Footprint to PAD_C8P0D2P8

20131121
Change H11 screw hole footprint from pad_ct6p0d4p3 to PAD_C6P0D4P3
Change H21 screw hole footprint from pad_ct5p5b8p0d2p5 to PAD_C6P0D2P8

20131121
Change H16 Footprint to PAD_CB6P0D2P8

20131121
Change footprint from PAD_CB5P0D4P0 to PAD_CT6P0B5P0D4P0

20131121
Delete H1 ,H2



PAD_C8P0D2P8



PAD_C8P0D2P8



PAD_CB8P0D2P8



PAD_C8P0D2P8



PAD_CT6P0B5P0D4P0



PAD_CT6P0B5P0D4P0



PAD_CT6P0B5P0D4P0



PAD_CT6P0B5P0D4P0



PAD_C6P0D4P3



PAD_C8P0D2P8

20131203
Change H13 Footprint to PAD_C9P0D7P6



PAD_C9P0D7P6

20131121
Delete H14



PAD_C8P0D2P8



PAD_C6P0D2P8



PAD_C8P0D2P8



PAD_ShapeT5P0X6P0-D



PAD_shapeT5P0X6P0-U



PAD_CB6P0D3P3



PAD_CB6P0D3P3



PAD_CT5P0B6P0D3P3



CHASSIS1_GND
PAD_C6P0D2P8

PCB Fedcal Mark PAD



GP1

PAD_RT2P65X2P2

@

GP2

PAD_RT2P65X2P2

@

GP7

PAD_RT2P65X2P2

@

GP8

PAD_RT2P65X2P2

@

GP11

PAD_RT2P45X2P5

@

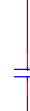
GP12

PAD_RT2P45X2P5

@

FFC CONN GROUND PAD

+VGA_CORE



+3VS




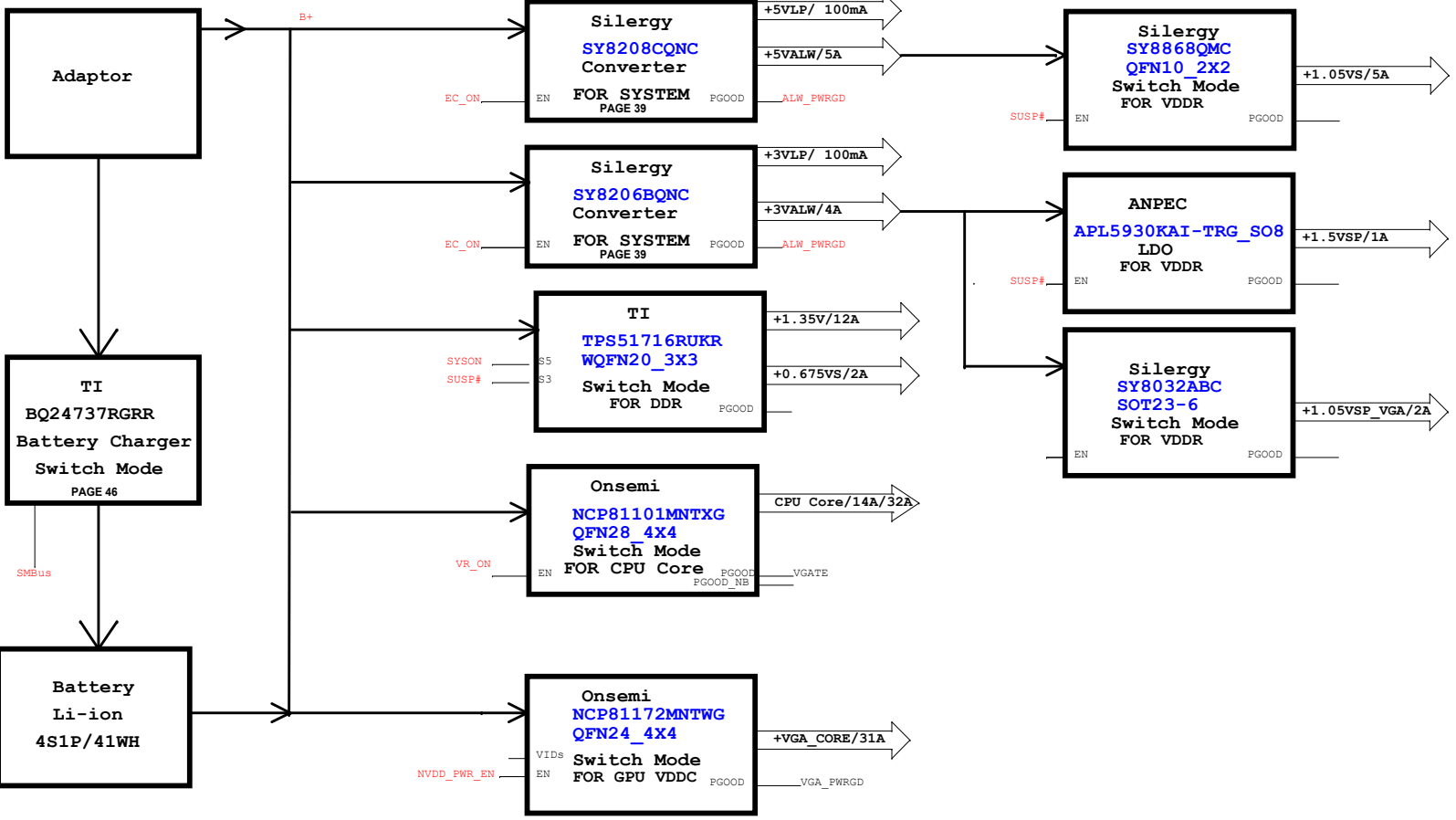
+5VALW

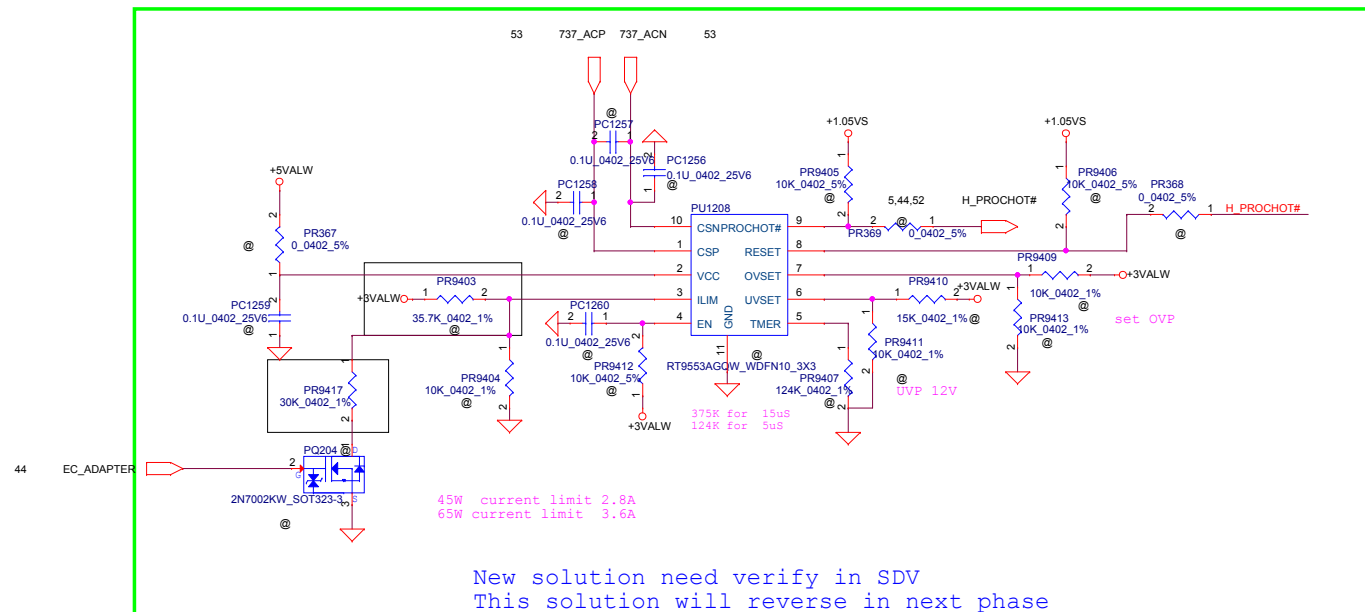
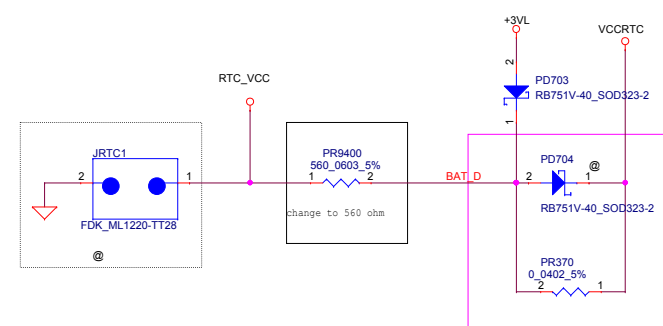
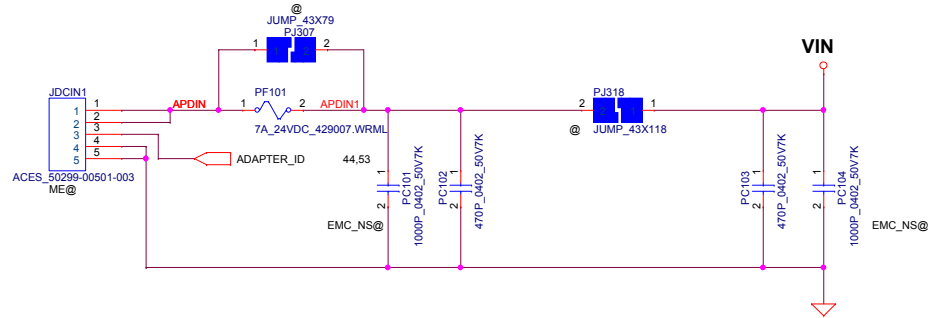


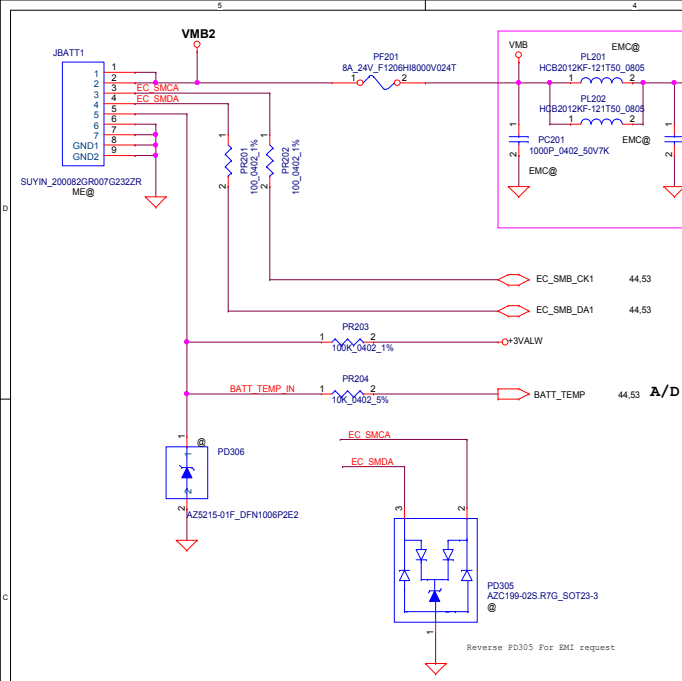
+3VALW

For EMC

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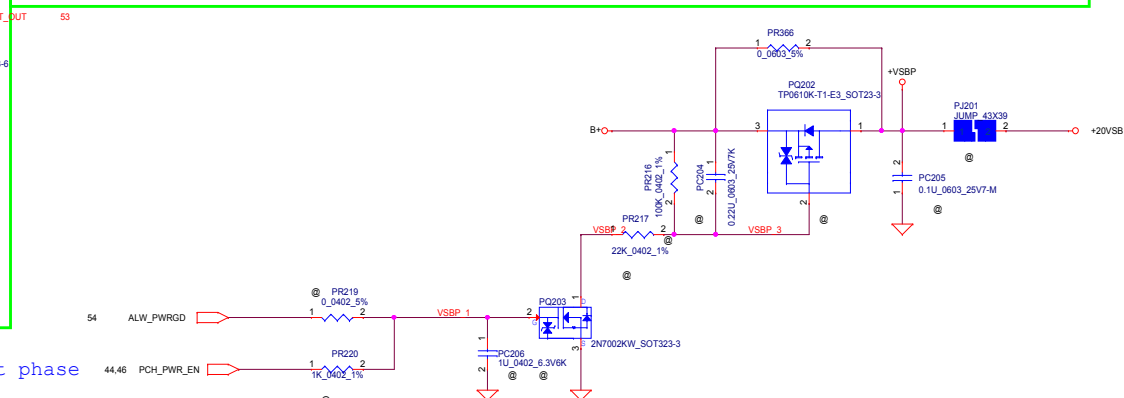
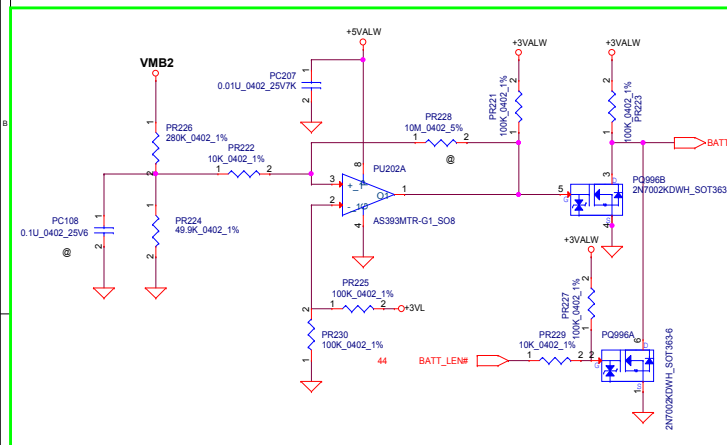
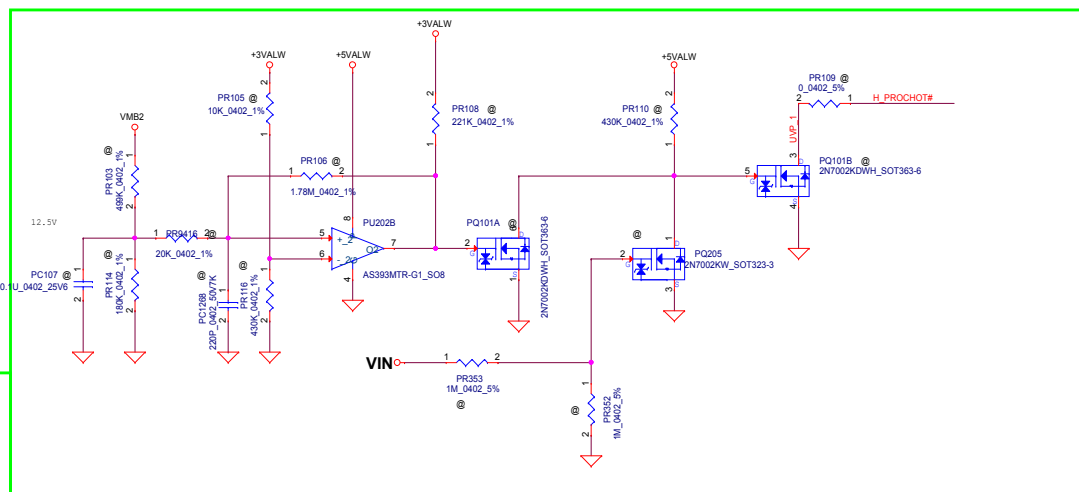
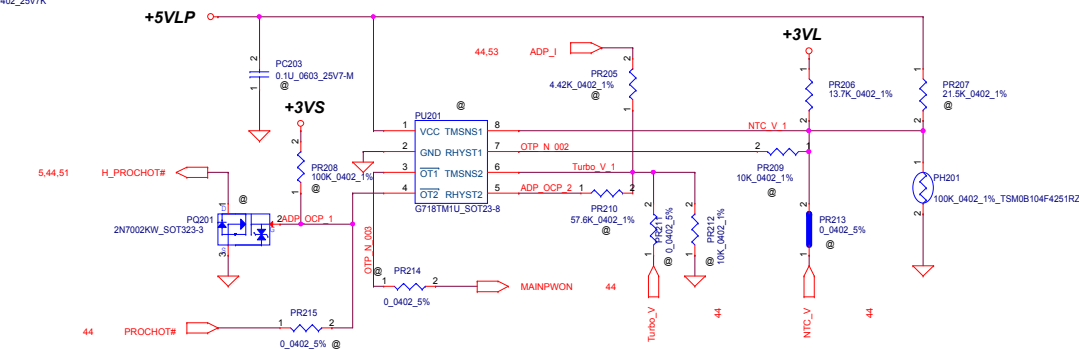






PH201 under CPU bottom side :
CPU thermal protection at 92+3 degree C
Recovery at 56 +3 degree C

For KB930 --> Keep PU1 circuit
(Vth = 0.825V)

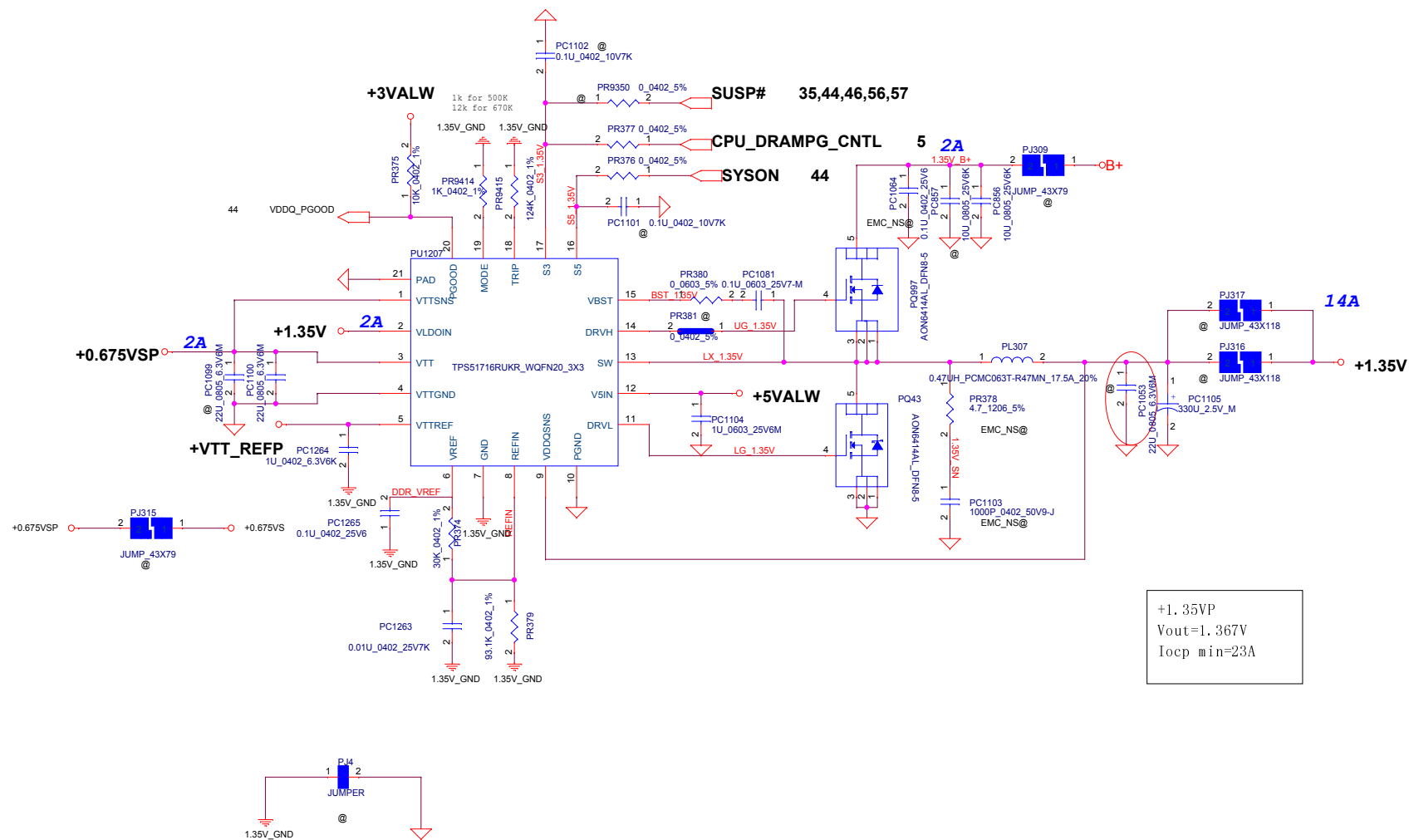
For KB9012 (Red square) --> Remove PU201 circuit, but keep PR206
PH201, PR205, PR211, PQ201, PR208, PR212



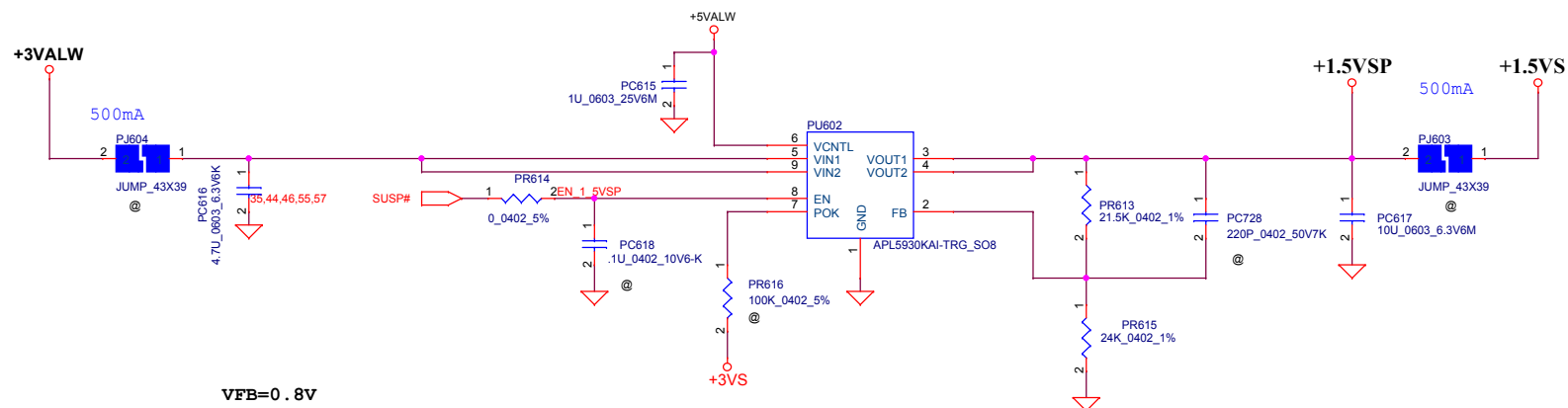
Use BATT_TEMP to implement BATT_OUT function,
New solution need verify in SDV, maybe can reverse in next phase


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Date:		Wednesday, July 16, 2014		Sheet		52 of 60		



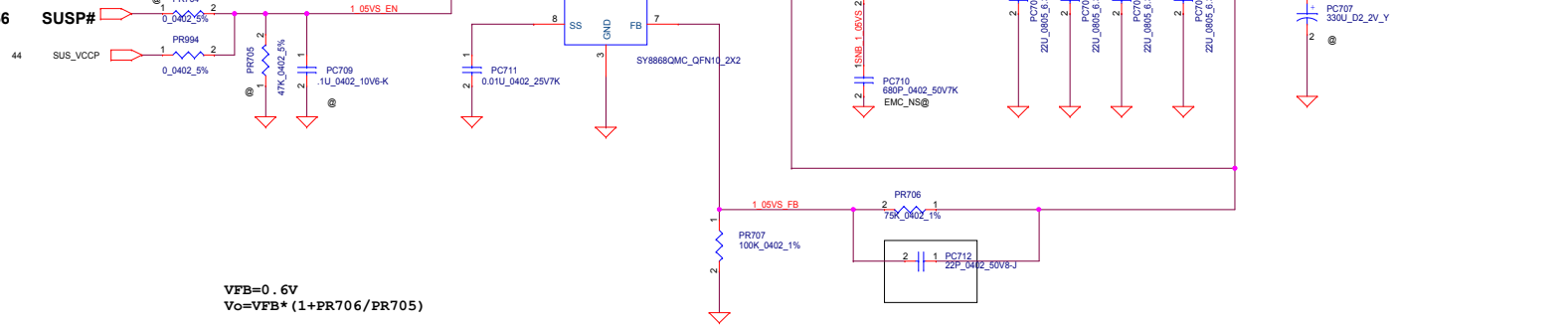


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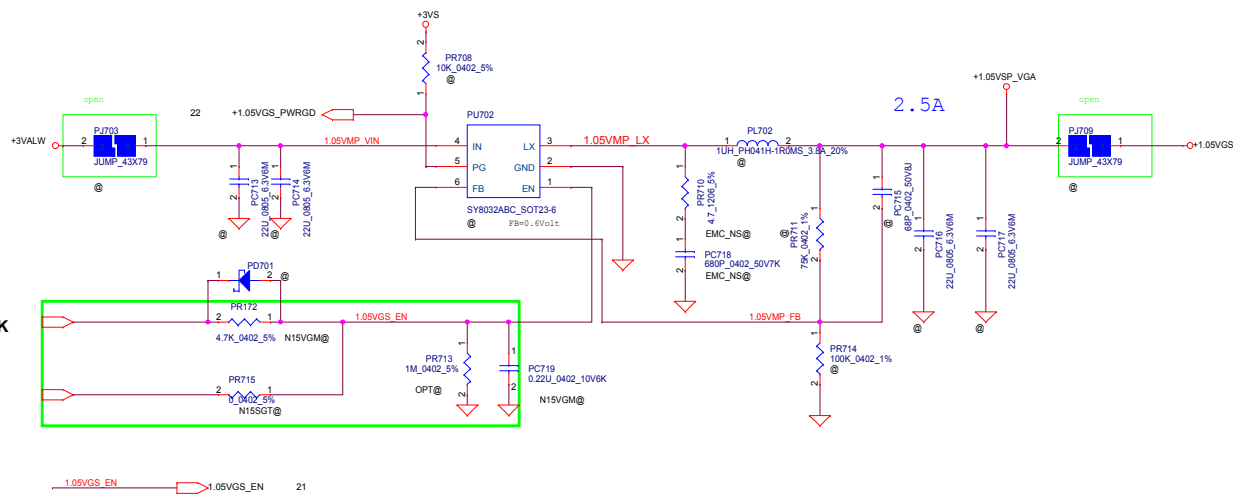
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35,44,46,55,56



23,58 DGPU_PWROK

22,58 EN_VGA



HW PIR (Product Improve Record)

BALG1/AIGL1/AILZ1 SCHEMATIC CHANGE LIST
REVISION CHANGE: 0.4
GERBER-OUT DATE: 2014/06/26

NO	DATE	PAGE	MODIFICATION LIST	PURPOSE
01)	06/22	21	Add virtual material CV54 0.1U	Follow N15V-GM Power rise time
02)	06/22	19	Add virtual material UV1 N15V-GM	Follow N15V-GM Power rise time
03)	06/22	07	Add virtual material YC1 Form SJ10000IM00 to SJ10000I300	HSW cost down
04)	06/22	03	Add BOM Structure Table list	HSW cost down
05)	06/26	45	Change L15 BOM structure form EMC@ to EMC_NS@	cost down
06)	06/29	04	Add virtual material UC1 BDW	Follow BDW CPU BOM structure
07)	06/29	04-13	Change UC1 BOM structure is HSW@	Follow HSW CPU BOM structure
08)	06/29	46	Change R159/R162 BOM structure is @	cost down
09)	07/09	21	Change RV59/RV64/RV72/QV10/QV13/QV20 BOM structure From OPT@ to @	cost down
10)	07/09	04	Change RC8 to PCB Short	cost down
11)	07/11	43	Change RA11 Pull high form +3VL to +3VS	follow G15
12)	07/11	07	Change QC3A/QC3B BOM structure is @	Cost down
13)	07/11	39	Change R176/R177 BOM structure Form UMA@ to PCB Short	Cost down
14)	07/17	45	Change D17 BOM structure Form EMC@ to EMC_NS@	Cost down
15)	07/17	45	Change QC3 BOM structure is @	Cost down